Date: Thu, 20 Oct 2011 10:11:55 -0500
From: Dan Michelson
To: Herb Johnson
Subject: Re: ZDS 1/40 Single Board Schematic Download

Herb,

Many years ago in 1983 I worked as an Electrical Engineer for a large company. We had dozens of ZDS 1/40's used for development. The 1/40 was a 4MHz version of the 1/20. Myself and another engineer decided to take the schematics of the 1/40 (from the Zilog manuals) and update them and create a single board version. We wanted to be able to have our own ZDS 1/40 system at home to do experimenting and we ended up doing several Z80 projects with the boards (we each had one). It was a big wire-wrap board connected to a pod, two 8" Shugart disks, a serial connector breakout board with two DB25's, a power supply, and a dumb terminal.

The schematic is 100% compatible with the original ZDS 1/40 unit. Note, CONN B was connected to a PCB from an existing system that we used to give us a connection to two DB25 connectors for the serial ports. These connection points could be replaced with DB9 connectors. It runs the same software, etc as the standard ZDS 1/40. At the time, we also convinced Zilog to give us all the source code for the ZDS 1/40 system since we thought we would have the units long after Zilog gave up support for them. I had the code on 8" hard sector disks and I transferred it to 5-1/4" disks. Several basement floods, and a lot of time, have apparently made them disappear so, unfortunately, I no longer have the source code. However I do still have the schematics for the wire-wrap we did.

The schematics were hand drawn on velum by myself and another engineer in 1983. They are a copy of the ZDS 1/40 schematics (and if I remember correctly, some updates to simplify using better circa 1983 parts) that consolidated all of the boards into one. The schematics have a connector that ties to the ribbon of the standard user pod (CONN A), and a connector for the serial ports (CONN B).

Looking at it now, the whole thing could be easily be put in an Altera or Xilinx FPGA using current external static memory devices in place of the dynamic 64KB memory, the CPU 2KB static memory, and the Trace 8KB static memory.

The schematic would be a good starting point to build a new version of the ZDS 1/40 emulator by integrating all of the logic in an Altera or Xilinx FPGA, removing the serial ports, removing the Floppy controller logic, and adding an Ethernet port (all inside the FPGA). The Z80 itself is available as IP from CAST Inc. for the Altera Cyclone series FPGA and can run at a speed of up to 82MHz. Essentially, the whole emulator could be upgraded significantly. The pod and the hybrid Z80 on the end of the Z80 in circuit emulator pod cable looks like it could also be easily duplicated in an FPGA. It would be a very interesting contrast to see such a re-designed system sitting side-by-side with the original ZDS 1/40.

The scanned drawings are at 600 dpi and grey scale, 11"X17", 22 pages.

Regards,

Dan Michelson

Sheet 1 - 4 is CPU2
sheet 5 is Memory 22
sheet 6 - 8 is Monitor 4.0
sheet 9 - 15 is Floppy Disk Controller
sheet 16 - 19 is Breakpoint
sheet 20 - 21 is RTSM2
sheet 22 is Comm

ISSUE
2-16-83

Z80A CPU

E&F 7

CPU 2

SHEET 1 OF

2E7 READ

CONNA 4Ø D0 41 D1 42 D2 43 D3 44 D4 45 D5 46 D6 47 D7

DIR OE LS245 F6

D0-D7 3B1,5C1 6B7,8B1 10E1,11D1 14A7,16B1 17D1,18A1 19C1,20A1 21B1,21D1

+5V 11 Vcc

D0 14 D1 15 D2 12 D3 8 D4 7 D5 9 D6 10 D7 13

4.7K 17 NMI

+5V 1K

MR PE CEP CET LS161 C4 QD QC

+5V 14 19.6608 OSC. C5 8 2 CK 7

4A1 5.1.238 MHz

POWER ON CLR 6E1,7C1 8A1,16E1

CONNA 4B1 22B1 Ø DRIVE

CONNA 39 POR (PSW)

7 RES SW N.C. 1 1K E8 +5V 16 1K E8 4 RES SW NO 2 5

E1Ø LS00 3 2 1 E1Ø LS00 6

D9 LS08 1 2 3

11 CONNA 61 INT 4E7 22E7 INT

49 WAIT 6B1 8B7 WAIT

51 BUSRQ

E9 LS244A 2 18 RESET 26

E9 LS244A 4 16 INT 16

E9 LS244A 6 14 WAIT 24

E9 LS244A 8 12 BUSREQ 25

BUSACK 23

GND 29

470 J11-12 470 J10-11 4.7K H5-6 +5V

A0 30 A1 31 A2 32 A3 33 A4 34 A5 35 A6 36 A7 37

OE1 OE2 LS244 E8

A8 38 A9 39 A10 40 A11 1 A12 2 A13 3 A14 4 A15 5

OE1 OE2 LS244 F8

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

A0-A15 2B1,2D1 2E1,3D1 5D1,5E1 7B1,17B1 21D1,4C1 22C1

RAMWR 5D1

CONNA A0 1 A1 2 A2 3 A3 4 A4 5 A5 6 A6 7 A7 8 A8 9 A9 10 A10 11 A11 12 A12 13 A13 14 A14 16 A15 17

RD WR IORQ MREQ M1 RFSH HALT 21 22 2Ø 18 27 28 18

OE1 OE2 LS244 E6

+5V 16 D6 4.7K

D8 LSØØ 8 9 10

RD 2E1,2C1,3C1,4B1,8B1,22B1 16D1

WR 3E1,4B1,22B1,7C1,16C1,2E1

IORQ 2D1,4B1,8B1,22B1

MREQ 2C1,5B1,16D1

M1 2E1,6E1,8C1,12Ø1,14C1,22C1 7A1

RFSH 5A1

HALT 6A1,12E1

CONTA RD 21 WR 22 IORQ 18 MREQ 67 M1 66 RFSH 65 HALT 48

+5V 16 4.7K 2 3 4 5 6 7 8 D6

BUSACK 2E1

BUSACK 5Ø

SYS PHI 71

POWER ON CLR 52

com Ø 22A1

ISSUE
2-16-83

7B7 PS2
7B7 PS3

+5V
C2-3 1K

C3 LS283
A12 A1
A13 A2
A14 A3
A15 A4
A0-A15 1B7
B1 B2 B3 B4 A1 A2 A3 A4 CO
Σ1 Σ2 Σ3 Σ4

A12+ 5E1
A13+ 5E1
A14+ 5E1
A15+ 5E1

C2 LS20
C9 LS32

MP15 3E1

1D7 MREQ
6E7 FORCE NOP
1D7 RD
1D7 WR
1D7 IORQ
1D7 M1
1D7 PODIEI
22B7 SYSMEM
C4 BUSACK

F9 F32
F10 LS00
D9 LS08
F10 LS32
J9 F02

G9 LS139
ENI ENZ A1 A0 Y0 Y1 Y2 Y3

G10 LS10
F13 LS32
C8 F21
F10 LS04
D8 LS08
H10 F10

8C7 IORQ·M1
1B7 A3
1B7 A2 IORD
3D7
1B7 A1
1B7 A0 RD

SEL

H9 LS00 8 MDIS 5B1
MEMRD 5B1

IACK 8A1
ROM 3C1
SRAM 3E1
CTCSEL 4B1
USART SEL 4B1
PORT FF 3C1
A0·A1 7B1
READ 1A1
MIORD 3A1
MIOEN 3A1

CPU 2

SHEET 2 OF

ISSUE
2-16-83

4C7 SI
2E7 MIOEN
2E7 MIORD

DØ-D7
1B1

IDØ-ID7
4D1
22D1

CONN.B
9 INT/NON-INT

2C7 ROM
2D7 PORTFF

8C7 IORQ-MY
1D7 RD

1D7 WR

2D7 SRAM

IORD
2D1,6B1,11B1
7C1

CPU2

SHEET 3 OF

ISSUE
2-16-83

1C1 S1.238MHZ

1K +5V H6-7

IEO1 22B1

1D7 WR
2D7 USARTSEL
1D7 RD
1C1 ΦDRIVE

2A9 +5V

1D7 IORQ
2D7 CTCSEL
1B7 A1
1B7 AΦ
1A8 INDX (ENA CLKΦ)
1D7 M1

CTC G6

CT3 2Φ
CT1 22

4.7K +5V G6-7

E1 E2

8251 G7

CONN B

RS232 DATA OUT 41
RS232 DATA IN 43
SI 3A1

7C7 SYS RESET
3B7 ID0-ID7
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7

INT 1D1

RESET 22E1

8,10,21,23,24,25,26,27,28,40,50 GND
+5V
31,32,33,34,35,36,37

CPU2

SHEET 4 OF

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	9-2-80	
2	2-16-83	

V_{CC} = +5V
V_{SS} = GROUND

mcm6665

MEMORY
25

APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR.	DSGNR.	
DRN.	DATE	

SHEET 5 OF

ISSUE
2-16-83

7E7 MONITOR
7E7 MONITOR
1D7 HALT
1D1 WAIT
J10 LS244 19
+5V
E18 1K
SENSE SW2
SENSE SW1
E14 LS244 OE1 OE2
CONNB
MONITOR LED 41
USER LED 42
HALT LED 40
WAIT LED 39
D1 D3 D4 D5 D6 D7
D0-D7
18I
16D7 BREAK STATUS
3D7 IORD
7A7 DEVFE
F13 LS32
CONNB
16 MONITOR SW N.O.
15 MONITOR SW N.C.
19 USER SW N.O.
18 USER SW N.C.
24 BREAK EMULATION
CONNA
F14 LS00
F16 F00
F15 F08
K18 LS04
CONNA
BREAK PENDING 7Φ
BREAK EMULATION 7D1
18E7 RUNB
7C7 SYS RESET
8B7 M1RQ
8D7 ΦB
1C1 POWER ON CLR
1D7 M1
+5V
1K E18
F74 G14
LS74 G15
H15 LS32
RESTARTD 2ΦA1
CHANGE MODE CLR 7C1
G16 F04
FORCE NOP DELAYED 2ΦA1 2A1
FORCE NOP 2C1
CONNA
FORCE NOP 6C8

MONITOR
4.0

SHEET 6 OF

ISSUE
2-16-83

1D7 M1

A0
A1
A2
A3
A4
A5
A6
A7
A0-A15
1B7

H10 F10 LS10
H12 LS32
LS155 G11
G10 LS10
G8 LS32
LS155 H11

2D7 A0·A1
8C7 IORQ·M1
1D7 WR
8C7 M1

SET MONITOR MODE (F7H)

DEV F8
DEV F9
DEV FA
DEV FB
DEV FC

DISK DATA 11B1
DISK CONTB 11B1
DISK CONTA 11A1
BKPT SEL 16E7
STOR SEL 20C1
DEV FE 6B1

(D8H) PS2 2A1, 22B1
(DCH) PS3 2A1, 22B1

H12 LS32
H12 LS32
IOWR 11A1

3D7 IORD
6D7 CHANGE MODE CLR
1C1 PWR ON CLR
6C7 BREAK EMULATION

G8 LS32
G8 LS32
SOFT RST
H10 LS10
H9 LS00
KA415
SYS RESET 4D1, 6D1, 14E1, 22D1
G10 LS10
F1 LS04
H9 LS00
H9 LS00
MON/USER

8B7 M1RQ

F74 H7
F74 H7
H8 LS04
CONNA
MONITOR 15
MONITOR 6A1
MONITOR 6A1

1K +5V
H9-10

8A7 M1S

MONITOR
4.0

SHEET 7 OF

ISSUE
2-16-83

1C1 POWER ON CLR
2C7 IACK
G3 FØ3
H4 LS02
J7 6306
J5 LS175 CK
J6 LS175 CK
D0-D7 1B1
M1S 7E1
M1S CONNA 19
J9 FØ2
M1RQ 6D1, 7E1 16A1
1D7 RD
1D7 IORQ
H12 LS32
IORQ·M1 2D1, 3C1, 7C1
1K HG-7 40
1D7 M1
J8 FØ4
J4 LS74
M1 7C1
J3 FØ0
CONNA
DATA STB 2ØB1, 21D1 18D1
ØB 6D1

MONITOR
4.0

SHEET 8 OF

ISSUE
2-1683

RX DATA
10B1, 12B1

14E7 RX MODE+

RXCLK
12C1

CONN C
READ DATA
4K
B1H2 470Ω
+5V
1 2

D12 LS74

D8 LS00

D8 LS00

1K
16 E18
10

B13 LS161
ENP LD
A B C D
CY
CK
CLR ENT

B13 LS04

16.589 MHz B15
8
27Ω
1K
+5V
+5V
+5

B14 LS93
Vcc GND
CLK
Qc 2Φ
QD
R1 R2

A 11E1

FLOPPY DISK CONTROLLER

SHEET 9 OF

ISSUE
2-1683

FD7
FD6
FD5
FD4
FD3
FD2
FD1
FDØ
FDØ-FD7
11D6

9A6 RX DATA

D14 LS95
D13 LS95
MODE
D15 LS173
C15 LS173
CLK
CL

12C7 SHIFT CLK
12B7 TX LOAD
11A5 READCHAR
12B7 RxBUFFLOAD

TXD 15C1
RCV DATA 15B1

DØ
D1
D2
D3
D4
D5
D6
D7
DØ-D7
1B1

FLOPPY DISK
Controller

SHEET 1Ø OF

ISSUE
2-1683

7C7 IOWR
7A7 DISK CONT A (DEV FA)
3D7 IORD
7A7 DISK CONT B (DEV F9)
7A7 DISK DATA (DEV F8)

B9 LS32 (1, 2, 3) → WR CONT1 → 14C1
B9 LS32 (4, 5, 6) → WR CHAR → 12E1, 13C1
B9 LS32 (9, 10, 8) → READ CHAR → 10E1, 13C1
B9 LS32 (12, 13, 11) → READ STATUS → 14B1
B8 LS32 (1, 2, 3) → WR CONT2 → 14E1
E15 F11 (1, 2, 13, 12)

D7 D6 D5 D4 → LS173 C14 (D1–D4 / Q1–Q4; CLK 7; CLR 15; IN 9; 10; 1, 2) → FD7 FD6 FD5 FD4

D3 D2 D1 D0 → LS173 A18 (D1–D4 / Q1–Q4; CLK 7; CLR 15; IN 9; 10; 1, 2) → FD3 FD2 FD1 FD0

D0-D7 1B1

FD0-FD7 → 10A1, 14D1

9E6 A → LS04 (4, 16; 9) → BA → 13E1

FLOPPY DISK CONTROLLER

SHEET 11 OF

ISSUE
2-16-83

START BIT

9 10 E16 LS08 8

14E7 WR MODE

9A6 Rx DATA

4 S 2 D C16 LS74 Q 6 R 1

SHIFT CLK 3 C

+5 5 VCC 10 GND

D16 LS93 QA QB 9 QC 8 QD 11 CB 1 R0 R1 2 3

1 2 E16 LS08 3 4 5 F16 F00 6

4 5 H15 LS32 6

TX BUFF UNLOAD → 13A1,15D1

11 B12 LS04 10 → TX LOAD → 1ΦC1

9 10 H15 LS32 8

RX BUFF LOAD → 1ΦC1,13A1

14E7 Rx MODE+ 1 2 B16 LS86 3

(RX+TX) → 13B1

6 B12 LS04 5

LS51

9B6 Rx CLK 2

13E7 Tx CLK 3

14B7 WR MODE+ 4

5 A16 16

4 5 B16 LS86 6

4 5 E16 LS08 6

SHIFT CLK → 1ΦC1,15B1

14E7 Rx MODE

+5 1K E1Φ-11

4 S 2 P Q 5 LS74 E11 C R 1

1A5 WR CHAR 9 B12 LS04 8 3

10 S 12 D Q 9 LS74 E11 11 C R 13

WRITE ENABLE → 15C1

FLOPPY DISK CONTROLLER

SHEET 12 OF

ISSUE
2-16-83

+5 — 1K — C17-18

12B7 Rx BUFF LOAD
12A7 Tx BUFF UNLOAD
C17 LS08

12C7 (Rx+Tx)
C17 LS08

C18 LS74

BUFF RDY
B15 LS05
WAIT 1D1

CHAR XFER

11A5 READ CHAR
11A5 WR CHAR
C17 LS08

A15 LS93

11E5 BA

15B7 Tx DB

C17 LS08

A17 LS20
A17 LS20
B17 LS00

CONN C
WR DATA 38

Tx CLK 12C1

FLOPPY DISK CONTROLLER

SHEET 13 OF

ISSUE
2-1683

CONN C

+5V

B12 13 · B13 4 · B14 15 · A14 15 · ALL 470Ω

22 RDY
42 TRK ØØ
44 WR PROT Ø
20 INDX Ø

LS 244

D7 D6 D5 D4 D3

DØ-D7 1B1

INDX 4C1

WR MODE+ 12D1, 15D1 CONN C

15B7 CRC ERR
11B5 READ STATUS

7406 B11

SEL Ø 26
SEL 1 28

7438 B1Ø

WRITE GATE 4Ø
STEP 36
DIRECTION 34
LOAD HEAD Ø 18

C1Ø LS175

4 D1 Q1 2 SEL Ø
5 D2 Q2 7
12 D3 Q3 10 MOTOR Ø
13 D4 Q4 15 MOTOR 1
9 CLK
R 1

11A5 WR CONT 1 (ØFAH)

C11 LS175

FD7 FD6 FD5 FD4
4 D1 Q1 2 WRITE
5 D2 Q2 7
12 D3 Q3 10 STEP IN
13 D4 Q4 15 STEP OUT
9 CLK Q1 3
R 1

FDØ-FD7 11D5

D11 LS175

FD3 FD2 FD1 FDØ
4 D1 Q1 2 HEAD
5 D2 Q2 7 Rx MODE
12 D3 Q3 10 CRC
13 D4
9 CLK Q2 6
R 1

11B5 WR CONT 2 (ØF9H)

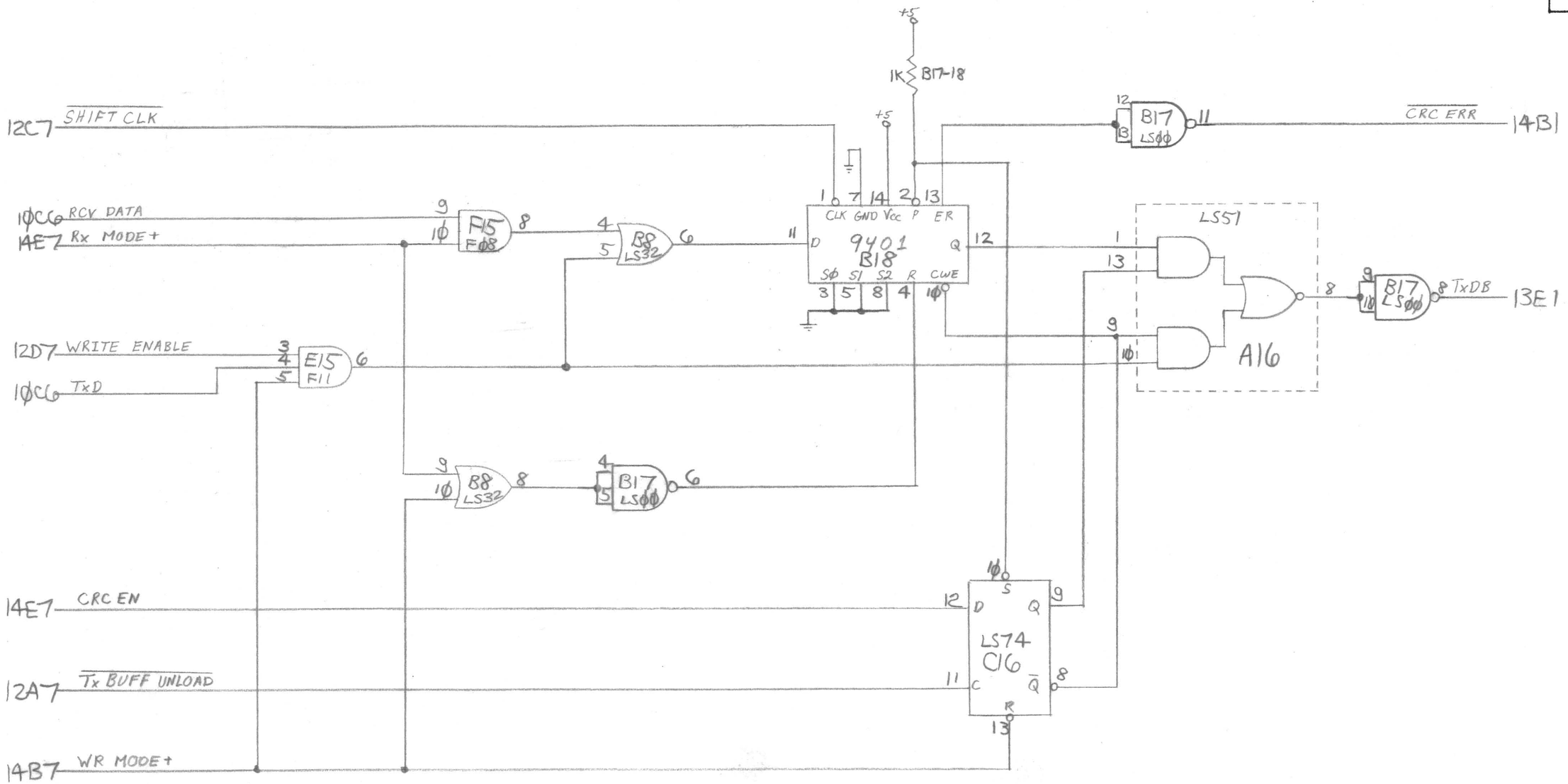
7C7 SYS RESET

WR MODE 12A1
Rx MODE+ 9B1, 12C1, 15B1
CRC EN 15D1
Rx MODE 12D1

FLOPPY DISK CONTROLLER

SHEET 14 OF

ISSUE
2-1683



FLOPPY DISK CONTROLLER

SHEET 15 OF

ISSUE
2-16-83

8B7 M1RQ

D0-D7 1B1

D4
D0 (IORD)
D1 (IOWR)
D2 (MRD)
D3 (MWR)
D5 (SYNC/BK)
D6 (DATA)
D7 (ADDRESS)

C1 LS374

A1

A3 LS32

B3 F08

H3 LS02 ×2

A5 F00

ENADDR LSB 17A1

IOWRB 2ØC1

IORDB 2ØC1

CONTROL EQ 17D1

CONTROL EQ 17D1, 18E1

D5 LS14

+5V

87-8 1K

B7 LS161

A5 F00

A5 F00

LOAD DATA 18D1
LOAD ADDR LOWER 17C1
LOAD ADDR UPPER 17C1
LOAD MASK 19B1

D B6 LS42

CONNA

53 HISIORQ

J9 F02

A4 LSØ2 ×3

1D7 WR
1D7 RD
1D7 MREQ

MRD 2ØB1
HISIORQ 2ØB1
MWR 2ØB1

B5 F151

1707 ADDR EQ
1807 DATA EQ
1707 BRK B

A5 F00

D10 LS02

18E7 RUN B
7A7 BKPT SEL
1C1 POWER ON CLR

H8 LS25

D9 LS08

+5V

J8-9 1K

G4 F00

G4 F00

BREAK STATUS 6B1

CONNA
BREAK 23
CONNB
SYNCBREAK 22

J8A LS04 ×2

BREAKPOINT

SHEET 16 OF

ISSUE
2-16-83

16A7 EN ADDR LSB

SA15
SA14
SA13
SA12
SA11
SA10

A9
A8
A7
A6
A5
A4
A3
A2
A1
A0

A0-A15
1B7

K14+15
LS244

SA15
SA14
SA13
SA12
SA11
SA10

SA10-SA15
2101

A1
F521

B1
F521

A3 F32
A3 F32
B3 F08

EQUAL

+5V
1K

16C7 LOAD ADDR LOWER
16C7 LOAD ADDR UPPER

A2
LS374

B2 LS374

D0
D1
D2
D3
D4
D5
D6
D7

D0-D7
1B1

F74
B4

ADDR EQ 16D1

B3 F08

F74
B4

BRK B 16E1

16B7 CONTROL EQ
18E7 BRK A
16B7 CONTROL EQ

18E7 RUN B

BREAKPOINT

SHEET 17 OF

ISSUE
2-16-83

DØ
D1
D2
D3
D4
D5
D6
D7

DØ-D7
1B1

G1
LS374
DØ ØØ
D1 Ø1
D2 Ø2
D3 Ø3
D4 Ø4
D5 Ø5
D6 Ø6
D7 CP
OE

16C7 LOAD DATA

G2 LS86
H2 LS86

DØ EQ
D1 EQ
D2 EQ
D3 EQ
D4 EQ
D5 EQ
D6 EQ
D7 EQ

DØEQ - D7EQ
19A1

1K +5V
K1-2

19B7 DATA BITS EQ
8D7 DATA STB

K2
LS74
D Q
CK
SD
CD

DATA EQ. 16E1

CONN A
2Ø RUN

16B7 CONTROL EQ

BRK A 17D1
RUN B 16E1, 17E1, 6D1
2ØC1, 21A1

BREAKPOINT

SHEET 18 OF

ISSUE
2-16-83

D0EQ
D1EQ
D2EQ
D3EQ
D4EQ
D5EQ
D6EQ
D7EQ
LOAD MASK
16C7

D0EQ-D7EQ
18C7

D0-D7
1B1

+5V
J1-2
47Ω

DATA BITS EQ 18D1

D0 3
D1 4
D2 7
D3 8
D4 13
D5 14
D6 17
D7 18

11 CP
1 OE
LS374
H1

D0 O0 2
D1 O1 5
D2 O2 6
D3 O3 9
D4 O4 12
D5 O5 15
D6 O6 16
D7 O7 19

J1 7438: 1, 2, 3
J1 7438: 4, 5, 6
J1 7438: 9, 10, 8
J1 7438: 12, 13, 11
J2 7438: 1, 2, 3
J2 7438: 4, 5, 6
J2 7438: 9, 10, 8
J2 7438: 12, 13, 11

BREAKPOINT

SHEET 19 OF

ISSUE
2-16-83

6D7 FORCE NOP DELAYED
6C7 RESTARTD

+5V
1K
DØ (IORD)
D1 (IOWR)
D2 (MRD)
D3 (MWR)
DØ-D7
1B1
LS175
CK
J16 LS00
J18 LS30
H17 LS04
D LS74 G18
SD
CD
LS08 H18
E18 1K +5V
J17 LS00
H18 LS08
WR DATA 21C1
6 ADD INC 21A1
16D7 MRD
16D7 MWR
HISIACK
8D7 DATASTB
16D7 HISIORQ
LS32
1D7 M1
16B7 IOWRB
16B7 IORDB
7A7 STOR SEL (DEVFC)
18E7 RUNB
J9 F02
J17 LS00
D0 D1 D2 D3 D4 LS374 OE
J16
MWRB 21E1
MRDB 21E1
IORDB 21D1
IOWRB 21D1
M1B 21E1
PE CEP CET MR LS161 CP J15
J17 LS00
A B C 2C 1G 2G LS155 J14
RD ADD LSB 21C1
RD ADD MSB 21C1
RD DATA 21C1
RD CONTROL 21C1
H15 LS32
READ
H17 LS04
WRITE LATCH EN 21E1

RTSM2

SHEET 2Ø OF

ISSUE
2-1683

18E7 RUNB
6D7 FORCE NOP DELAYED
2ΦB7 ADD INC

J11 LS169 TC
J12 LS169 TC
J13 LS169
RA0 RA1 RA2 RA3 | RA4 RA5 RA6 RA7 | RA8 RA9 RA10

J12-3 1K +5V

1B1 D0-D7

H5 LS244
K4-5 LS244
K1 LS244
H14 LS244

E12 2Φ16
E13 2Φ16
G12 2Φ16
G13 2Φ16

2ΦC7 RD ADDR MSB
2ΦC7 RD ADDR LSB
2ΦC7 RD DATA
2ΦC7 RD CONTROL
2ΦB7 WR DATA

E17 LS374
F17 LS374
G17 LS374

8D7 DATA STB

17A7 SA0-SA15
1B7 A0-A9
1B1 D0-D7
2ΦB7 IORDB
2ΦB7 IOWRB
2ΦB7 MRDB
2ΦB7 MWRB
2ΦC7 M1B
1B7 HALT

6G2 SBUSACK

K18 LS244

F12 LS74
F12 LS74

1K

2ΦE7 WRITE LATCH EN

RTSM2

SHEET 2 OF

ISSUE
2-16-83

IE5 COMΦ

1K +5V F17-18

F18 CK LS74

1D7 WR
7B7 PS3
1D7 RD
1C1 ΦDRIVE
4A7 IEO1

1D7 IORQ
7B7 PS2
1B7 A1
1B7 AΦ

1D7 M1

C12 CTC

+5V

7C7 SIS RESET

IDΦ ID1 ID2 ID3 ID4 ID5 ID6 ID7
IDΦ-ID7 3B7

4D7 RESET

C13

KA615 LS14A

CONN A
PODIEI 63
PODIEI 2E1

CONN B
TxD 1
RxD 3
RTS 2
CTS 4
DSR 5
DTR 6

D17 1488
D18 1489

INT 1D1

Comm

SHEET 22 OF