

82S181 8K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S181 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181 is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 90ns max
- Input loading: $-150\mu\text{A}$ max
- On-chip address decoding
- Four chip enable inputs
- Four chip enable inputs
- Outputs: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

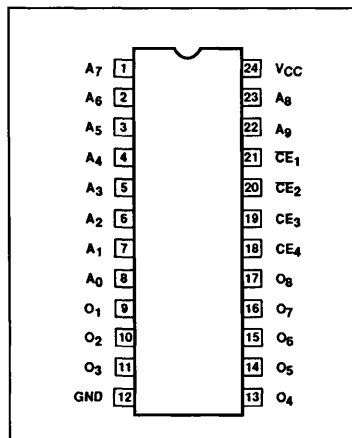
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 600mil-wide	82S181/BJA
24-pin Ceramic Flat Pack	82S181/BKA
28-Pin Ceramic LLCC	82S181/B3A

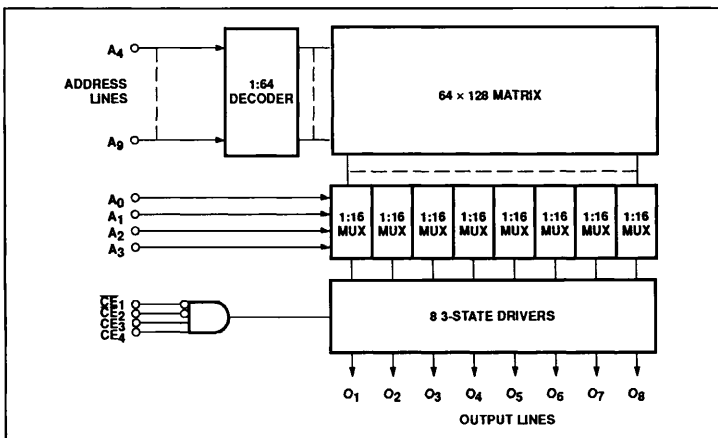
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-65 to +150	$^{\circ}\text{C}$

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (1024 × 8)

82S181

DC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
			Min	Typ ⁵	Max	
Input voltage²						
V_{IL} V_{IH} V_{IK}	Low High Clamp	$V_{CC} = 4.5\text{V}$, $I_I = -18\text{mA}$	2.0		0.8 -0.8 -1.2	V V V
Output voltage²						
V_{OL} V_{OH}	Low High	$V_{CC} = 4.5\text{V}$ $\overline{CE}_{1,2} = \text{Low}$, $CE_{3,4} = \text{High}$ $I_O = 9.6\text{mA}$ $I_O = -2\text{mA}$	2.4		0.5	V V
Input current¹						
I_{IL} I_{IH}	Low High	$V_{CC} = 5.5\text{V}$ $V_I = 0.45\text{V}$ $V_I = 5.5\text{V}$			-150 40	μA μA
Output current¹						
I_{OZ} I_{OS}	Hi-Z state Short circuit	$V_{CC} = 5.5\text{V}$ $\overline{CE}_{1,2} = \text{High}$, $CE_{3,4} = \text{Low}$, $V_O = 5.5\text{V}$ $\overline{CE}_{1,2} = \text{High}$, $CE_{3,4} = \text{Low}$, $V_O = 0.4\text{V}$ $\overline{CE}_{1,2} = \text{Low}$, $CE_{3,4} = \text{High}$, $V_O = 0\text{V}$ $V_{CC} = 5.5\text{V}$, High stored	-15		40 -40 -85	μA μA mA
Supply current						
I_{CC}		$\overline{CE}_{1,2} = \text{High}$, $CE_{3,4} = \text{Low}$, $V_{CC} = 5.5\text{V}$		125	185	mA
Capacitance⁶						
C_{IN} C_{OUT}	Input Output	$\overline{CE}_{1,2} = \text{High}$, $V_{CC} = 5.0\text{V}$ $V_I = 2.0\text{V}$ $V_O = 2.0\text{V}$		5 8	10 13	pF pF

AC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ⁵	Max	
t_{AA}	Access time ⁴	Output	Address		50	90	ns
t_{CE}	Access time ⁴	Output	Chip Enable		20	50	ns
t_{CD}	Disable time	Output	Chip Disable		20	50	ns

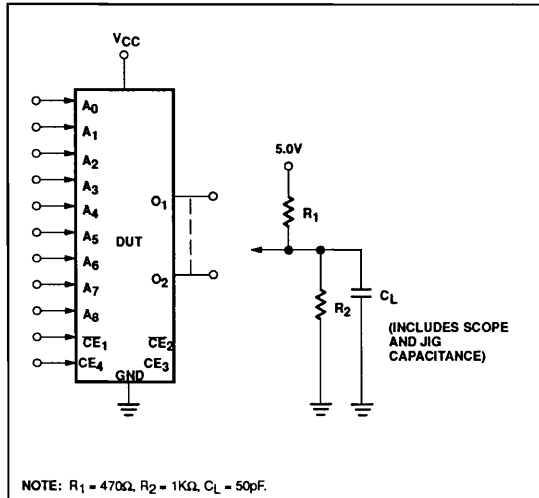
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of $1\mu\text{s}$.
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = +25^{\circ}\text{C}$.
6. Guaranteed, but not tested.

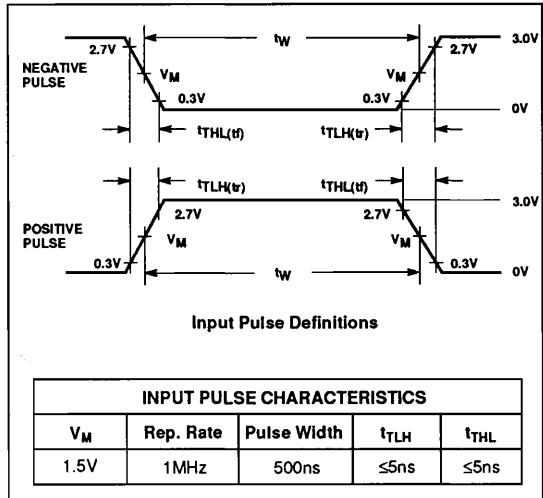
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TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



TIMING DIAGRAMS

