Ipso Facto

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The purpose of this article is to present information to assist in the independant use of the 57109 Number Oriented Processor that is an integral part of the NETRONICS FULL BASIC package.

Background

Like many others, I find FULL BASIC to be extremely limited except for its excellent math capability made possible by the 57109. It naturally follows that the use of the 57109, independant of BASIC should be helpful.

The following narrative,subroutines and examples should assist anyone to make use of this tool in their programming. It is assumed that anyone interested in this subject has the National Semiconductor Data Sheet on the 57109 that was included in the NETRONICS' package. Except for the interfacing, the Data Sheet contains all information needed to use the 57109.

INPUT

All numbers and commands are entered from memory to the math processor (MP) via an OUTPUT 5 (65) instruction. Do this by setting RX to the address of the byte to be input and issue the 65 instruction or set X to the PC and issue a 65 instruction immediately followed by the byte to be input.

The MP requires all numbers and commands to be 2 digits. Each of the 2 digits is in octal notation and only contains 3 bits. However, these 2 octal digits are moved from memory into the MP as a single hexadecimal byte where the 2 high order (leftmost) bits are insignificant. eg., to input the number 1 into the MP,"01"octal must be fed in as 6 bits- 000 001. This must represented in memory as hex "01" or 0000 0001.Straight forward so far,but to input the command "Master Clear", 57 octal must be fed in as- 101 111. This is represented as 0010 1111 or 2F.

Exhibit A is a list of all numbers and commands in hex.

The MP must be synchronized with the 1802 by a delay between each input byte. This delay is accomplished by issuing INPUT 2 instructions until the proper response is received. See the subroutine "I/P Delay".

OUTPUT

Results can be obtained from the MP and put into memory by issuing 2 OUT instructions (16). The first of these instructions is followed by an input delay and the second is followed by an output delay. The output delay is a loop that continues until EF2 = 1. When EF2=1, the MP is ready to output results which can be put into memory by issuing an INPUT 2(6A) instruction either 10 or 12 times depending on whether the MP is in Floating Point (FP) or Scientific Notation (SN) mode respectively. Each 6A instruction must be followed by an output delay.

Each 6A instruction places a byte in memory. The high order nibble of each byte is a 9 which is meaningless and can be eliminated. If the MP is in FP mode, the first output byte identifies the sign (90=+,98=-) and the second byte identifies the position of of the decimal point in the mantissa. This requires manipulation as a 9B indicates the decimal should be placed immediately after the most significant mantissa digit and decrements until 94 indicates the decimal is after the least significant digit. The 8 mantissa digits follow from most to least significant.
If the MP is in SN mode, the first output byte is the most significant exponent digit and the second byte is the least significant exponent digit. The third output byte contains the sign of both the exponent and the mantissa (the 8 and the 0 bits). The fourth byte is the decimal point location which is always 9B and is not needed. The 8 mantissa digits follow.

SUBROUTINES

To illustrate the above, two subroutines are included in exhibits B and C. Both routines utilize a standard call and return technique (SCRT) that always resets X to 2 on a D4 or D5.

The input subroutine is called by D4 XX00 and is followed by a string of numbers or commands in hex notation as shown in exhibit A. The string is terminated by an FE. If an FF byte is encountered in the string, the next two bytes must contain an address where from 1 to 8 numerical bytes are stored followed by either a plus sign (2B) or a minus sign (2D). The string continues after the 2 byte address until an FE or another FF is encountered.

The output subroutine is called by D4 XX3B and is followed by three bytes. The first identifies the number of decimal places that are wanted in the final result (from 00 to 08) and the next two are the address of the final 9 byte answer (8 digits plus a sign). This output routine is used for floating point only and assumes that the MP has not been toggled into SN mode.

The output subroutine first dumps 10 bytes into memory at XXF0-XXF9 while changing the high order nibbles from 9 to 3. Eight bytes of memory at the designated location are zeroed and the sign is stored. The number of decimal places wanted in the final answer is calculated and the result in ASCII is moved to the final location.

SCIENTIFIC NOTATION

It is important to realize that all processing takes place internally in scientific notation mode. The TOGGLE command (22) changes mode from FP to SN and vice-versa. The MCLR command (2F), in addition to resetting all MP registers, places the MP in in FP mode. EE (0B) may be issued with the MP in either mode and does not TOGGLE.

The TOGGLE command only affects the size and format of the results from the MP.

The full results of the MP when in SN are 12 bytes, not 10 as in the attached subroutines.

EXAMPLES

Assuming that you entered the code from exhibit B and C into page XX of memory, enter following into some other page:

00	D4XX00	Call Input
03	2F	Master Clear
04	01 02 03 39	123+
08	02 02 3B	22X
0B	FE	Terminate Instruction
0C	D4XX3B	Call Output
0F	00	No decimal consideration
10	YYYY	Address of final answer
12	3012	

Execute and YYYY should equal 30 30 30 30 32 37 30 36 2B
or 123+ 22X = 2706+

Now enter

00	D4XX002F	Call Input and MCLR
04	FFYYYY	Enter numbers at YYYY until a 2B or 2D
07	2134	Enter and √ Commands
09	01020A020539	12.25+
0F	FE	Terminate instruction
10	D4XX3B	Call Output
13	02	Allow 2 decimal places in final answer
14	YYYY	Address of final answer
16	3016	

Execute and YYYY should equal 30303030363432362B or 2706√ 12.25+ = 64.26+

HEX	Numbers	HEX	Commands	HEX	Commands
00	0	21	Enter	38	Y^x
01	1	39	+	37	1/x
02	2	3A	-	34	$\sqrt{\ }$
03	3	3B	X	33	Square
04	4	3C	÷	32	10X
05	5	2F	MCLR	31	EX
06	6	2B	ECLR	35	LN
07	7	16	OUT	36	LOG
08	8	27	SF1	24	SIN
09	9	28	PF1	25	COS
0A	.	29	SF2	26	TAN
0B	EE	2A	PF2	2D	DTR
0C	CS	22	TOG	2C	RTD
0D	π	23	ROLL	1C	MS
		2E	POP	1D	MR
3F	NOP	30	XEY	1E	LSH
		1B	XEM	1F	RSH

2 WORD COMMANDS

20 39 M+
20 3A M-
20 3B MX
20 3C M÷

57109 Commands in HEX

EXHIBIT A

SUBROUTINE : INPUT TO MATH PROCESSOR CALL: D4 XX00 ssssss...FE Terminates
FF followed by 2 byte addres

```
00  E6              Start    SEX 6      Set X to Link
01  06FBFE321A               Test for FE- Yes, RETURN
06  FB013210                 Test for FE- Yes address follows
0A  65D4XX1C                 Input String- Call IP Delay
0E  3000                     Branch to Start
10  1646BA46AA       Addr    Input from memory- load RA from link
15  D4XX22                   Call Inpmem
18  3000                     Branch to Start
1A  16D5             Ret     Main Return
1C  6A7E7E           IP Delay Input Delay Subroutine
1F  3B1C
21  D5
22  EA0A             Inpmem  Input memory subroutine
24  FB2B3221                 If + Return
28  FB063293                 If - Change sign then Return
2C  0AFA0F5A                 Zero high nibble
30  65D4XX1C                 Input byte from memory- Call IP Delay
34  3022
36  0000000000               No meaning
```

EXHIBIT B

SUBROUTINE : OUTPUT FROM MATH PROCESSOR CALL: D4XX3B BB AAAA
BB= No. of decimal places AAAA= Address

```
3B  F80AAC                  RC= No. of characters from MP
3E  93BDF8F0AD              RD= Address of scratch work area
43  46AB46BA46AA            Link load RB.0 and RA
49  E36516D4XX1C            Issue OUT command- Call IP Delay
4F  E36516                  Issue second OUT command
52  3D52          OP Delay  Output delay - Loop until OP ready
54  ED6A                    OP ready- put byte in memory
56  F0FA0FF9305D            - There is time for this processing
5C  1D2C                    - before going to
5E  8C3A52                  - OP Delay
61  F808AD                  All MP results are npw in work area
64  F8305A                  Zero area before storing final answer
67  2D1A8D3A64
6C  F8F0AD                  Point RX to sign
6F  F0FB30328F                is it +?
74  F82D5A2A      Sign      Store - sign
78  1DF83C                  Point RX to decimal point
7B  F7AC                    Calc no. in integer
7D  8BE252                  Calc total no. in answer-
80  8CF4AC                    store in RC.0
83  FCF1AD
86  EA0D73        Move      Move answer from work area to
89  2C2D                      final location
8B  8C3A87
8E  D5            Ret       Main Return
8F  F82B          +         Store + sign
91  3076
93  E3650C        CS        Change sign- from Input subroutine
96  D4XX1C                  Call IP Delay
99  D5                      Return
```

EXHIBIT C

RCA News

RCA/Solid State Division
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Three new CMOS video interface IC's from RCA enchance video and graphics display capabilities of the CDP1800 microprocessor. The Video Interface System Chip Set features black-and-white, gray scale and color graphics and motion on a 40x24 character display. The chip set also features programmable line and dot colors and offers a variety of formats for video/graphics display and modification under software control, with either NTSC or PAL compatible output signals. The chip set has hardware-scroll capability and provides a sound output of white noise and eight octaves of programmable tones, variable in 16 steps from 0 to 0.78 VDD.

For further information on the VIS Chip Set, including data File No. 1197 and application note ICAN-7032, write to RCA Solid State Division, Box 3200, Somerville, NJ 08876, or call Memory/Microprocessor Marketing at (201) 685-6206.