

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}^1	To Program	$I_{CCP} = 350 \pm 50\text{mA}$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S^3	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25\text{V}$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5\text{V}$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4\text{V}$			-500	μA
Output Voltage						
V_{OUT}^2	Output Programming Voltage	$I_{OUT} = 200 \pm 20\text{mA}$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1\text{V}$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_p	$\overline{\text{CE}}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0\text{V}$	5			sec
T_{PR}^4	Programming Duty Cycle				33	%
$T_{PR} + T_{PS}$						

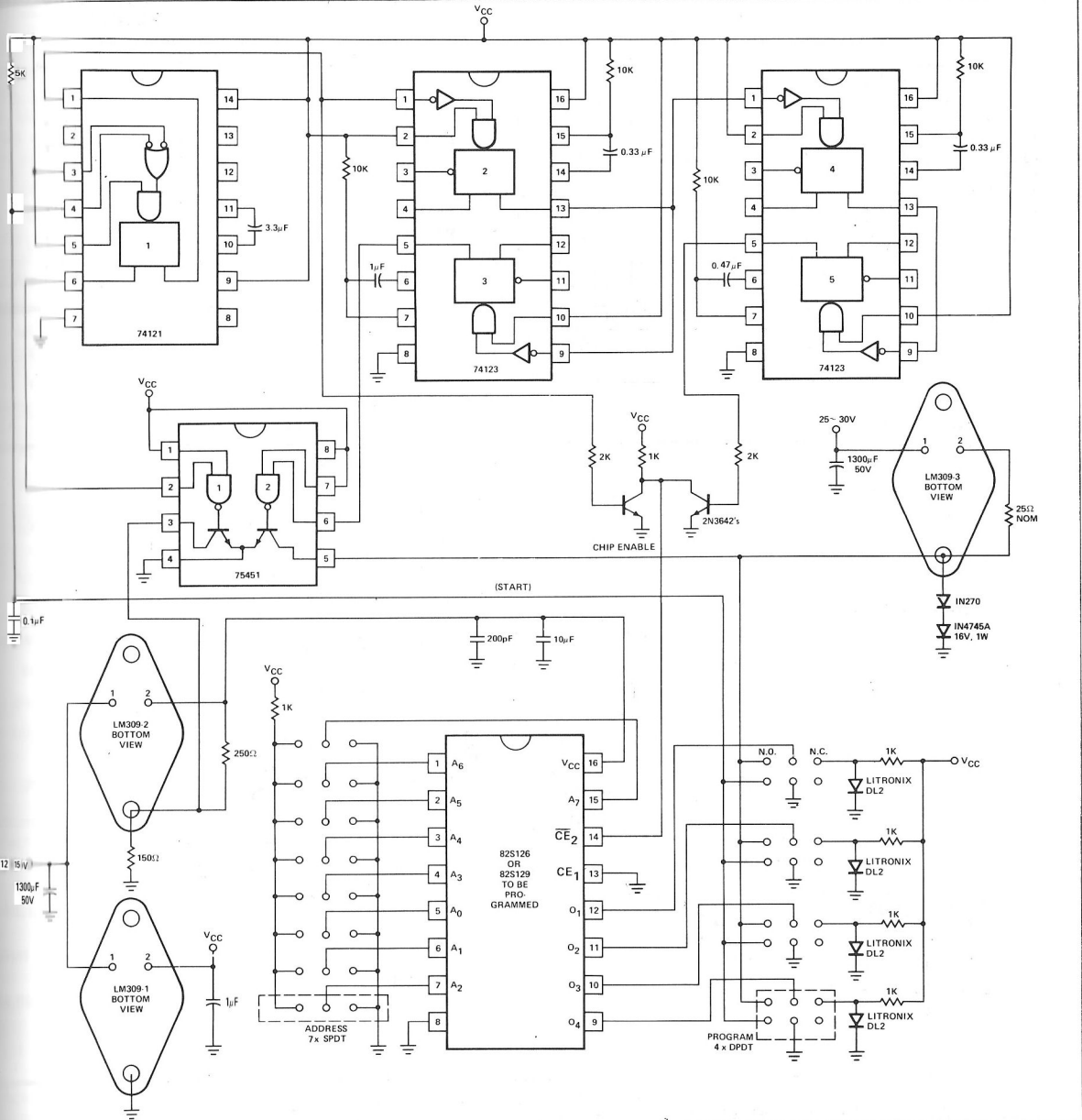
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10\text{K}\Omega$ resistor to V_{CC} .
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$.
3. After $10\mu\text{s}$ delay, apply $V_{OUT} = +17 \pm 1\text{V}$ to the output to be programmed. Program one output at the time.
4. After $10\mu\text{s}$ delay, pulse both $\overline{\text{CE}}$ inputs to logic "0" for 1 to 2 ms.
5. After $10\mu\text{s}$ delay, remove +17V from the programmed output.
6. To verify programming, after $10\mu\text{s}$ delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$, and apply a logic "0" level to both $\overline{\text{CE}}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$, and repeat steps 3 through 6 to program other bits at the same address.
8. After $10\mu\text{s}$ delay, repeat steps 2 through 7 to program all address locations.

NOTES:

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing temp.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a fusing cycle ($V_{CC} = 0\text{V}$) of 4ms.

MANUAL PROGRAMMER



TIMING SEQUENCE

