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THE MICROPROCESSOR-BASED MAGSAT COMMAND SYSTEM

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ABSTRACT

A microprocessor-based command system has been designed, tested, fabricated, and flight qualified for integration into the MAGSAT spacecraft for the remote execution of relay, pulse, and data commands. Limited semiautonomous operations in conjunction with attitude, power, and telemetry systems are featured. A stored memory of 2.8 kilobytes in CMOS PROMS with 1 k bytes of random access CMOS memory provide the program and the working space for the microprocessor to decode command messages. The design represents the first in a new generation of command systems for satellites designed at APL and offers expanded user capabilities, increased flexibility in real time, and delayed command operations.

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ILLUSTRATIONS

1. BACKGROUND

The MAGSAT satellite is being developed by APL under contract with NASA to provide an accurate survey of the earth's magnetic field. The scaler and vector magnetometer data provided by the satellite will be processed by the U.S. Geological Survey to update and refine the magnetic charts for 1980. Magnetic crustal anomalies will be investigated for potential discoveries of various natural resources. NASA's Goddard Space Flight Center will also process the data to update mathematical models of the magnetic field of earth caused by internal current systems.

The two basic units of the MAGSAT spacecraft, the base module and the instrument module, can be seen in the orbital configuration shown in Fig. 1. The extended boom, with the sensor platform, houses the vector, scaler magnetometers, and a precision sun sensor and is an integral part of the instrument module. The other primary subsystems in the instrument module are the optical bench, which contain two star cameras, and the attitude transfer system. The base module contains the majority of the satellite electronics including the command system.

One of the basic constraints in the MAGSAT program was the budgetary consideration, which required the use of spare flight hardware from SAS-C (the third in a series of small astronomy satellites launched from Africa in 1975). Indeed, the initial proposal for the MAGSAT command system included a reproduction of the proven SAS-C command system design in order to integrate the two SAS-C spare power switching modules and the spare redundant command converters. However, the new NASA command uplink, along with other pertinent considerations, led to a new command system design.

The microprocessor era began in the early 1970's with the introduction of a 4-bit controller circuit by Intel. This led to the 4-bit microprocessor, Intel's 4004 chip. The 4004 integrated circuit (IC) began a revolution in the electronics industry that has yet to be fully realized or comprehended. Four-bit microprocessors soon grew to 8-bit microprocessors, which are now being replaced by 16-bit circuits. In parallel with the growth of the microprocessor, memory circuits, which are required for support, kept pace. It is ironic that the first microprocessors were introduced primarily to sell memory chips — which is still true today — although the basic cost in a microprocessor-based system lies with software development. Today, the industry is testing

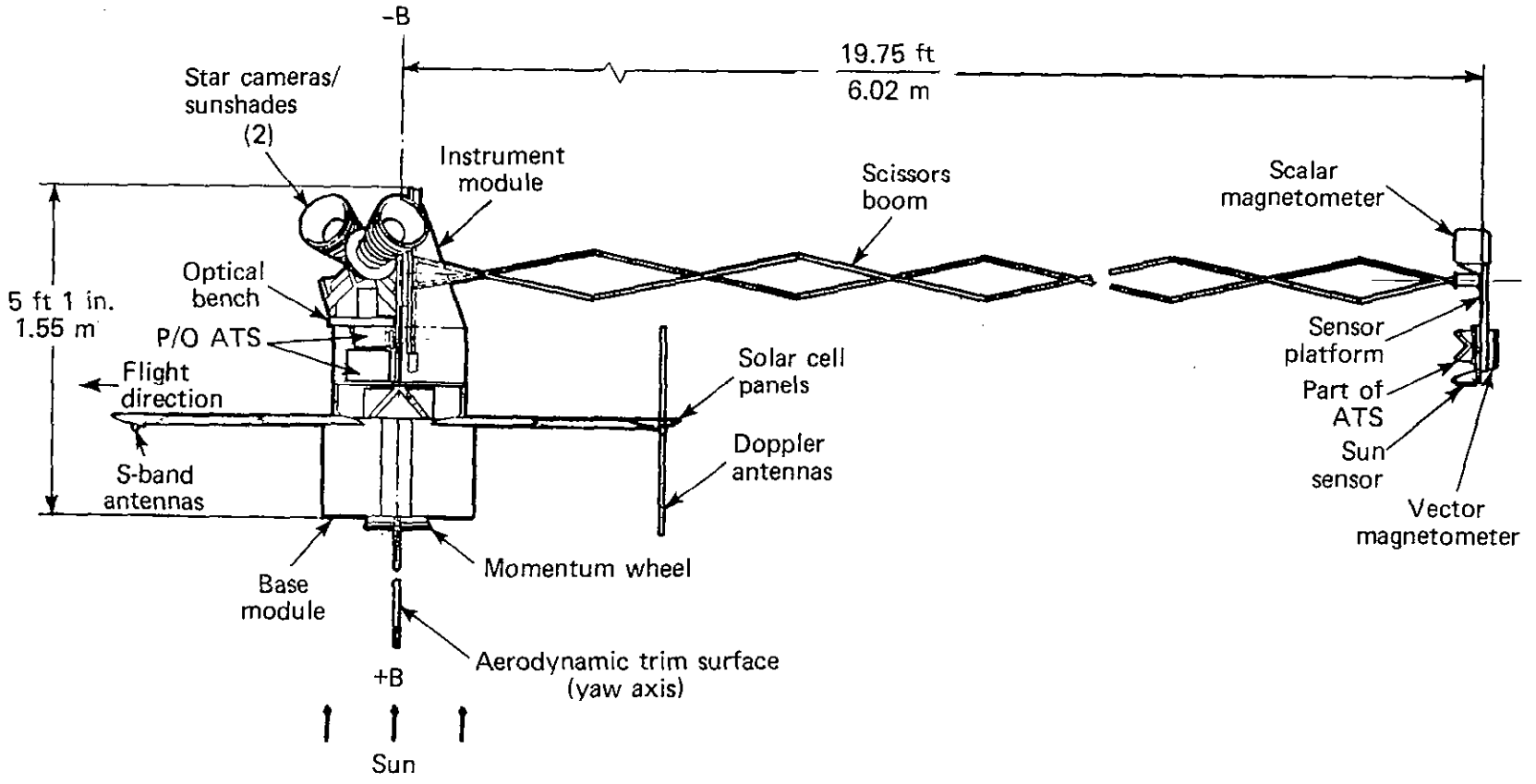

Fig. 1 MAGSAT orbital configuration, top view.

64 k-bit random access memory (RAM) circuits. Indeed, the microprocessor is well on its path to ubiquity in future electronic systems.

Design of the MAGSAT command system began in the summer of 1977. When the first controllers were introduced in the early 1970's, microprocessors had matured to the point where the alternatives of microprocessor-based versus random logic designs had to be considered in the design of complex spacecraft electronics. Such a comparison resulted in the selection of a microprocessor-based design. Three families of circuits were considered for the design: two NMOS families (the Motorola 6800 microprocessor and the Intel 8080 microprocessor) and the RCA 1802 CMOS microprocessor.

The RCA CMOS 1802 microprocessor family of circuits was selected and supported with small-scale integration (SSI) and medium-scale integration (MSI) CMOS circuits because of the following considerations:

1. Power Consumption. The power used by any system on board a spacecraft parametrically ripples through the design of the power subsystem and imposes various thermal constraints. The RCA 1802 CMOS technology is power efficient by two orders of magnitude compared to the NMOS microprocessors.

2. Existing Command Converters. The existing SAS-C command converters generate +20, -10, and +5 V. There is enough current available in the +5 V line to support a CMOS procesor design, whereas NMOS designs would impose a current drain well beyond the capability of the SAS-C +5 V line.

3. Radiation Effects. Although radiation hardening was not the paramount factor in the MAGSAT design, it was a strong consideration. All known hardening programs at the time of selection involved the 1802 IC's. It was prudent to select a potentially hard family that could also be integrated into other APL space programs.

4. General Considerations. (a) Static CMOS circuitry, (b) simpler clock circuitry, (c) wide temperature tolerance, and (d) single power supply operation.

2. DISCUSSION

COMMAND SYSTEM

Figure 2 is a block diagram of the command system. Exclusive of the S-band antenna, this system incorporates full addressed redundancy. Two government-furnished NASA Standard Transponder-Near Earth (NST-NE) receivers process the uplink 16-kHz subcarrier modulation and output command data to its respective command processor for decoding to execute the following types of command functions:

1. Relay Commands. The power switching modules execute the relay contact closures to perform 56 power and signal switching commands.

2. Data Command (Short). Twenty-four user-defined bits of information are routed to the selected destination.

3. Data Command (Long). Loads of variable lengths are executed for delayed commands within the command system, and a fixed 768-bit load can be sent to the attitude processor.

4. Pulse Commands. Command pulses are generated for the operation of relays contained in the various MAGSAT subsystems. The pulse commands handle those MAGSAT functions that were not accommodated by the existing SAS-C power switching modules.

All command functions can be executed on either a real-time or a delayed basis with the exception of the long-data load. Additionally, each command processor is programmed for limited semiautonomous operations with the telemetry and attitude subsystems.

Multiple-command execution is a feature of the design. The command-message stream (Fig. 3) consists of a 128-bit (minimum) checkerboard preface followed by an 8-bit sync word, a real-time command message limited to a maximum of 2048 bits (the equivalent of 32 real-time commands), and the trailing 16-bit checkerboard. The message can be composed of any combination of real-time command frames or long-data loads. Long data loads must be prefaced by an introductory command (64-bits) and is thereby constrained to 1984 load bits, which could be representative of a sequence of 31 delayed commands. Typical command frame microstructures are shown

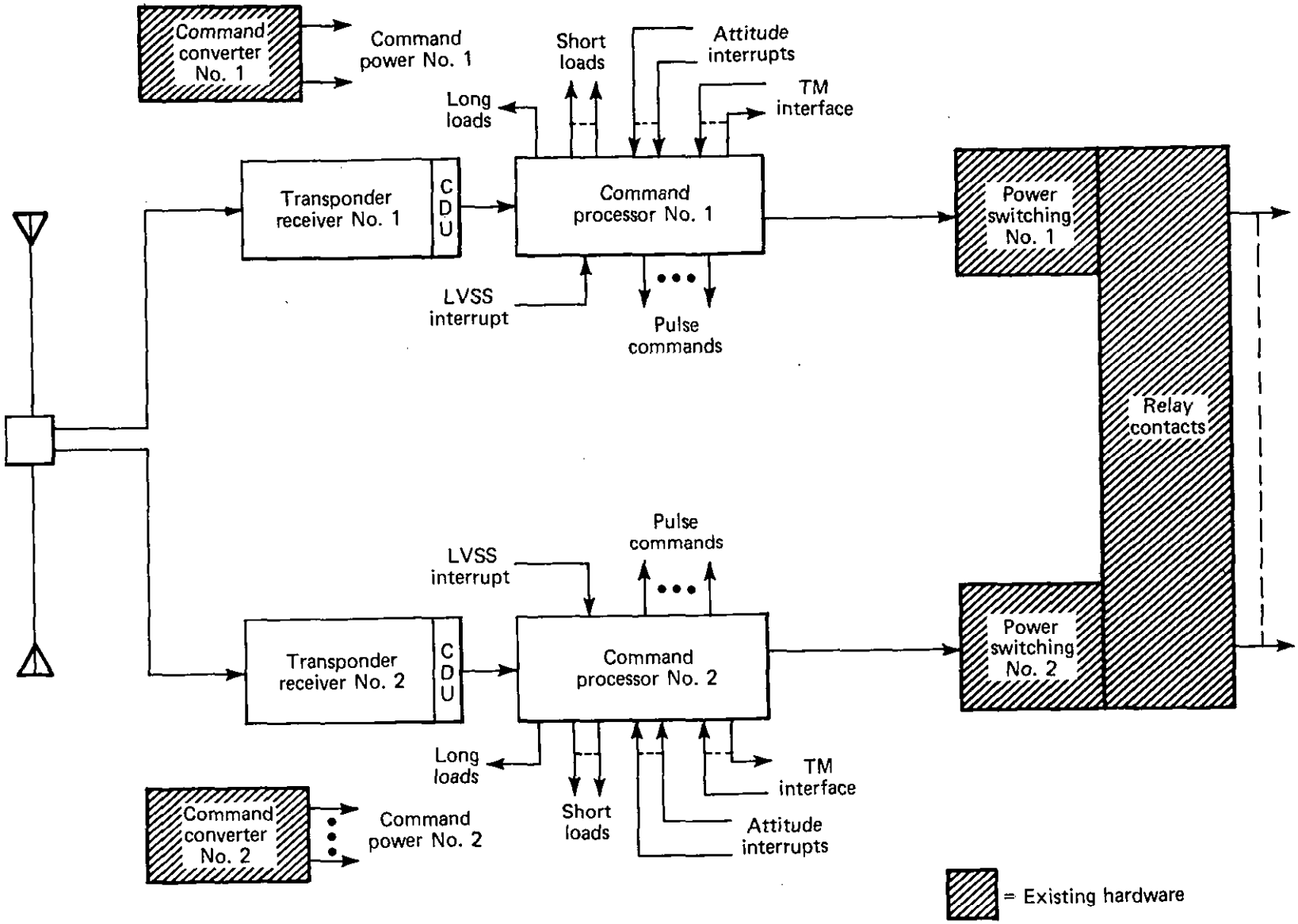

Fig. 2 MAGSAT command subsystem.

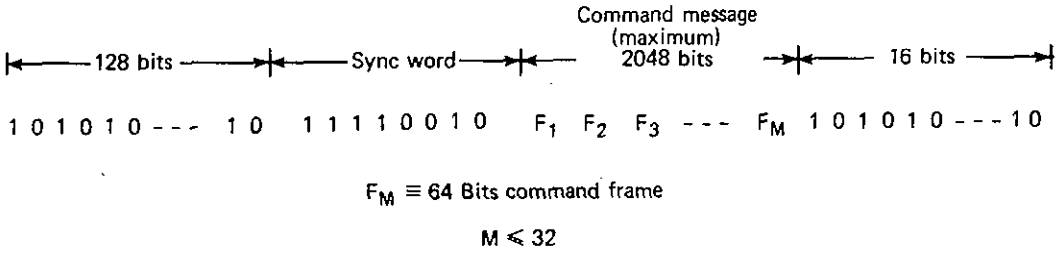

Fig. 3a Command message stream.

Byte	1st	2nd	3rd	4th	5th	6th	7th	8th	
Real-time relay	$A_7 \ldots A_1 L_2$	$L_1 000X \ldots X$	$N_8 \ldots N_1$	$X \ldots X$	$X \ldots X$	$X \ldots X$	$IR_6 \ldots R_1 X$	$H_7 \ldots H_1 X$	
Delayed relay	$A_7 \ldots A_1 L_2$	$L_1 100X \ldots X$	$N_2 N_1 E_{14} \ldots E_9$	$E_8 \ldots E_1$	$X \ldots X$	$X \ldots X$	$IR_6 \ldots R_1 X$	$H_7 \ldots H_1 X$	
Real-time long load	$A_7 \ldots A_1 L_2$	$L_1 011 D_4 \ldots D_1$	$N_8 \ldots N_1$	$X \ldots X$	$M_{16} \ldots M_9$	$M_8 \ldots M_1$	$K_8 \ldots K_1$	$H_7 \ldots H_1 X$	Load bits→

Fig. 3b Typical command frames.

in Fig. 3b. All command frames must specify satellite address, processor select, and command-type bits in the first two bytes. Since multiple commands are allowed, byte 3 of the first command frame in the real-time sequence must specify the number of commands in that sequence. All command frames must specify a truncated Hamming error detection code in the eighth byte.

For real-time relay commands, byte 7 selects the relay command for execution. For delayed relay commands, bytes 3 and 4 specify the delayed timing for each delayed command cluster with the number of delayed commands (four maximum) per cluster defined by N_2N_1 of the third byte. For the long-load command, the introductory command specified the starting address (bytes 5 and 6) and byte count (seventh) for the storage of the ensuing load bits.

Both command processors will operate on the uplink command message; however, only one processor will be selected to execute the desired command function. The processors will normally be in the main mode of the general polling routine shown in Fig. 4. The general polling routine samples the following flags to determine the desired command operation: (a) real-time commands, (b) low-voltage commands execution, (c) delayed commands, (d) attitude maneuvers, and (e) automatic S-band transmitter power turn off. The general polling routine can be interrupted for the loading of the bit stream of the real-time command message.

Upon sensing a real-time interrupt and with the successful detection of checkerboard and sync, the command sequence is loaded in a working area in the RAM memory space for processing by the general polling routine. Real-time commands will be processed accordingly for either relay, pulse, short-data (24 data bits), or long-data (memory load commands). Delayed command sequences will be extracted from the working RAM space and loaded into the delayed command RAM space. The delayed command's storage area can accommodate up to five different sequences totaling 82 commands. Each sequence is composed of command clusters with each cluster containing up to four commands, as noted in Fig. 5. After each delayed command load, an automatic telemetry (TM) readout is generated for subsequent ground-station load verification. This request will initiate the dedication of the TM system for verification at the next minor TM frame.

Additionally, there is a command to the command system itself to read out a specified area in command memory for up to 256 bytes. There are provisions for defeating this dedication for an anomaly in this interface. With confirmation, an epoch set command for the designated delayed load will start the processing of the delayed commands. For extended delayed command operations, there is a capability for linking different delayed command loads.

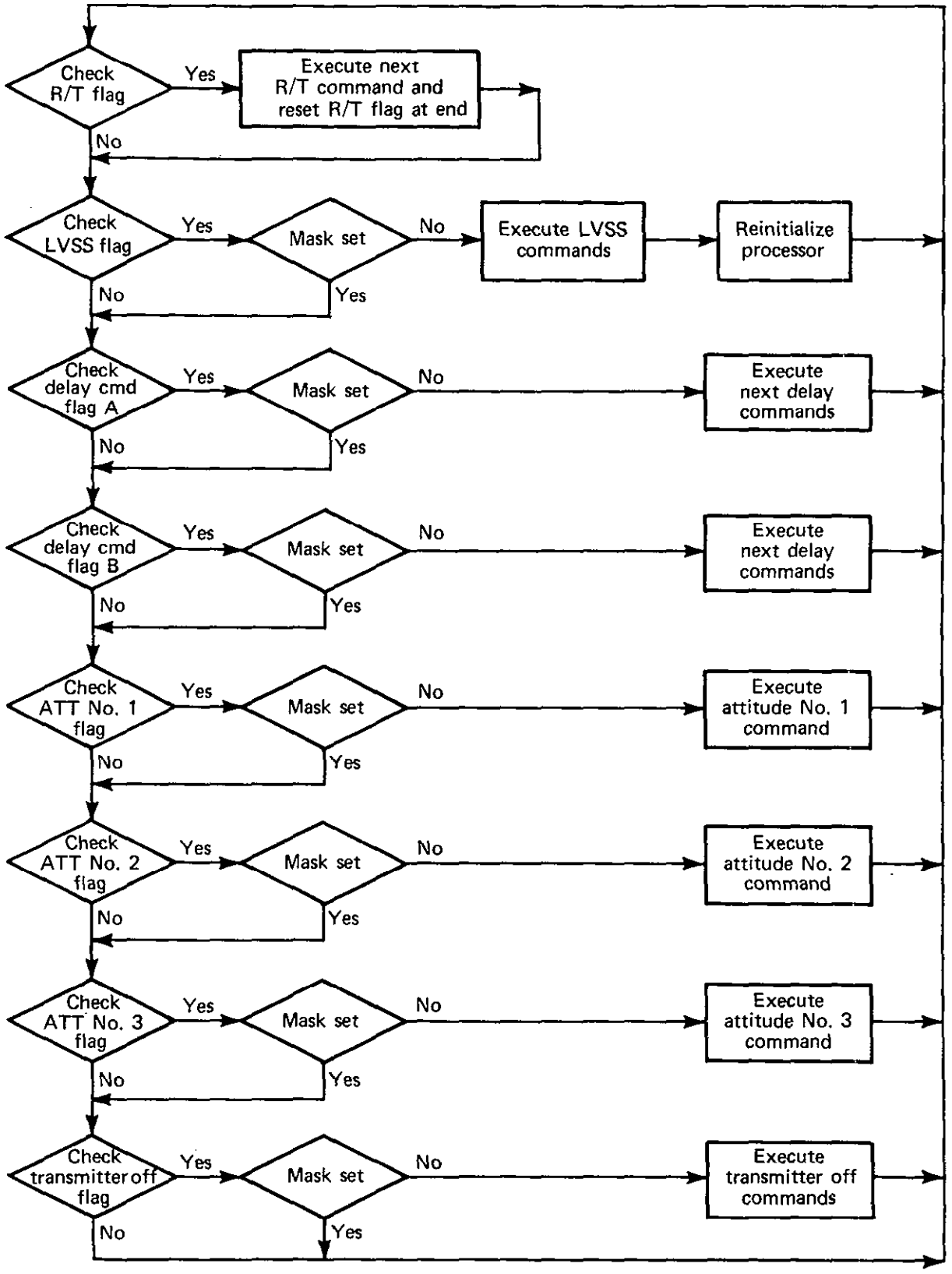

Fig. 4 General polling scheme for MAGSAT command.

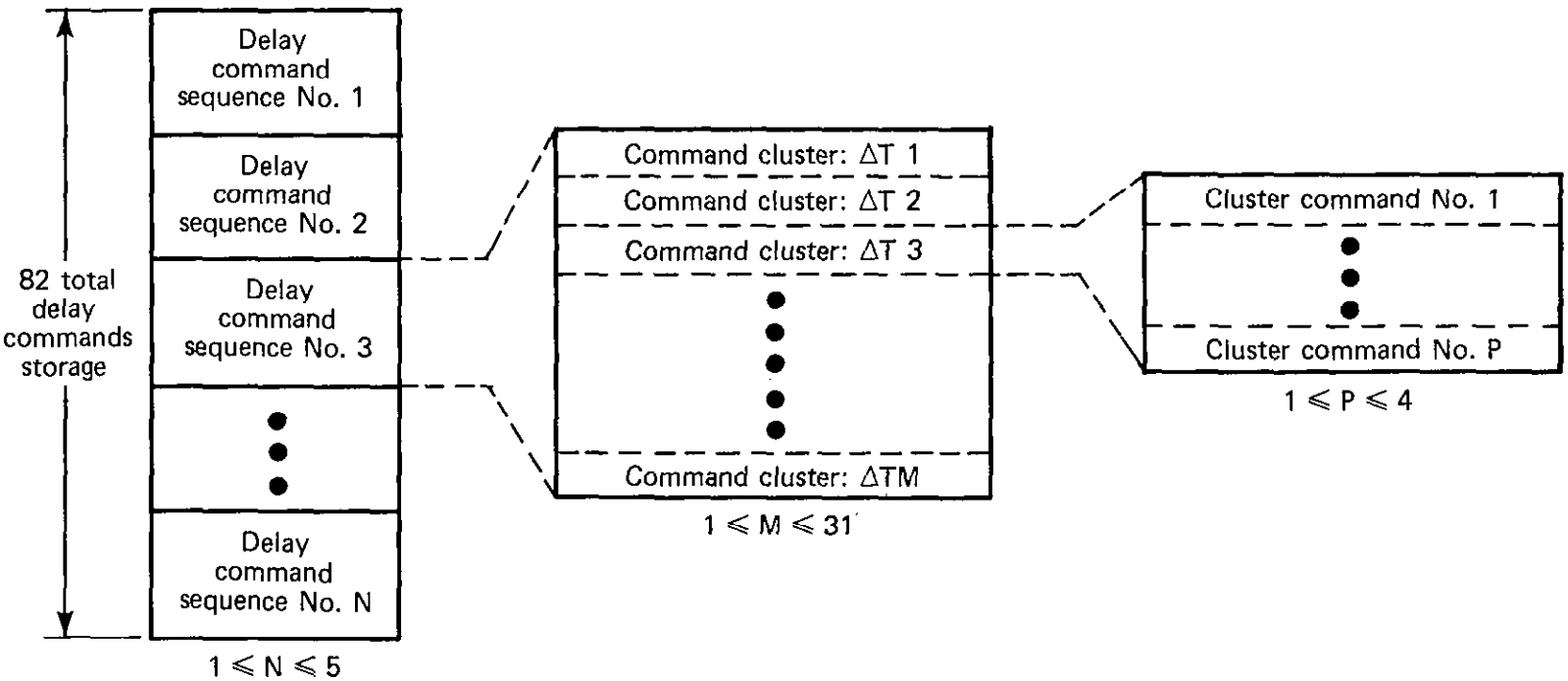

Fig. 5 Delayed commands RAM space allocation.

PHYSICAL DESCRIPTION

Physically, the command system is packaged in two units, each containing a command processor and its respective SAS-C power switching module (Fig. 6). When integrated into the MAGSAT structure, the two command units are separated by two gyro books. Pertinent weight and volume statistics are listed in Table 1.

Each command module dissipates 280 mW at nominal voltages. Both processors normally execute the general polling routine and await interrupts for command functions. Processing of the various functions does not significantly change the power consumption.

Communications with other systems are via connectors. Power switching is output from each module exit via a 288-pin Hughes connector. Pulse and data commands are handled via two 88-pin connectors from each command processor assembly. Finally, there is a 51-pin test connector on each processor book for monitoring the microprocessor.

Table 1

Physical characteristics of command system

	Weight		Volume
Command module 1	Command processor	2.79 lb (1266 g)	6.25 by 6.25 by 3.125 in. = 122 in^3 (16 by 16 by 8 cm = 2048 cm^3)
	Power switching	3.16 lb (1433 g)	6.25 by 6.25 by 2.125 in. = 83 in^3 (16 by 16 by 5.4 cm = 1382 cm^3)
Command module 2	Command processor	2.83 lb (1284 g)	6.25 by 6.25 by 3.125 in. = 122 in^3 (16 by 16 by 8 cm = 1382 cm^3)
	Power switching	2.88 lb (1306 g)	6.25 by 6.25 by 2.125 in. = 83 in^3 (16 by 16 by 5.4 cm = 1382 cm^3)
	Total	11.66 lb (5289 g)	410 in^3 (6860 cm^3)

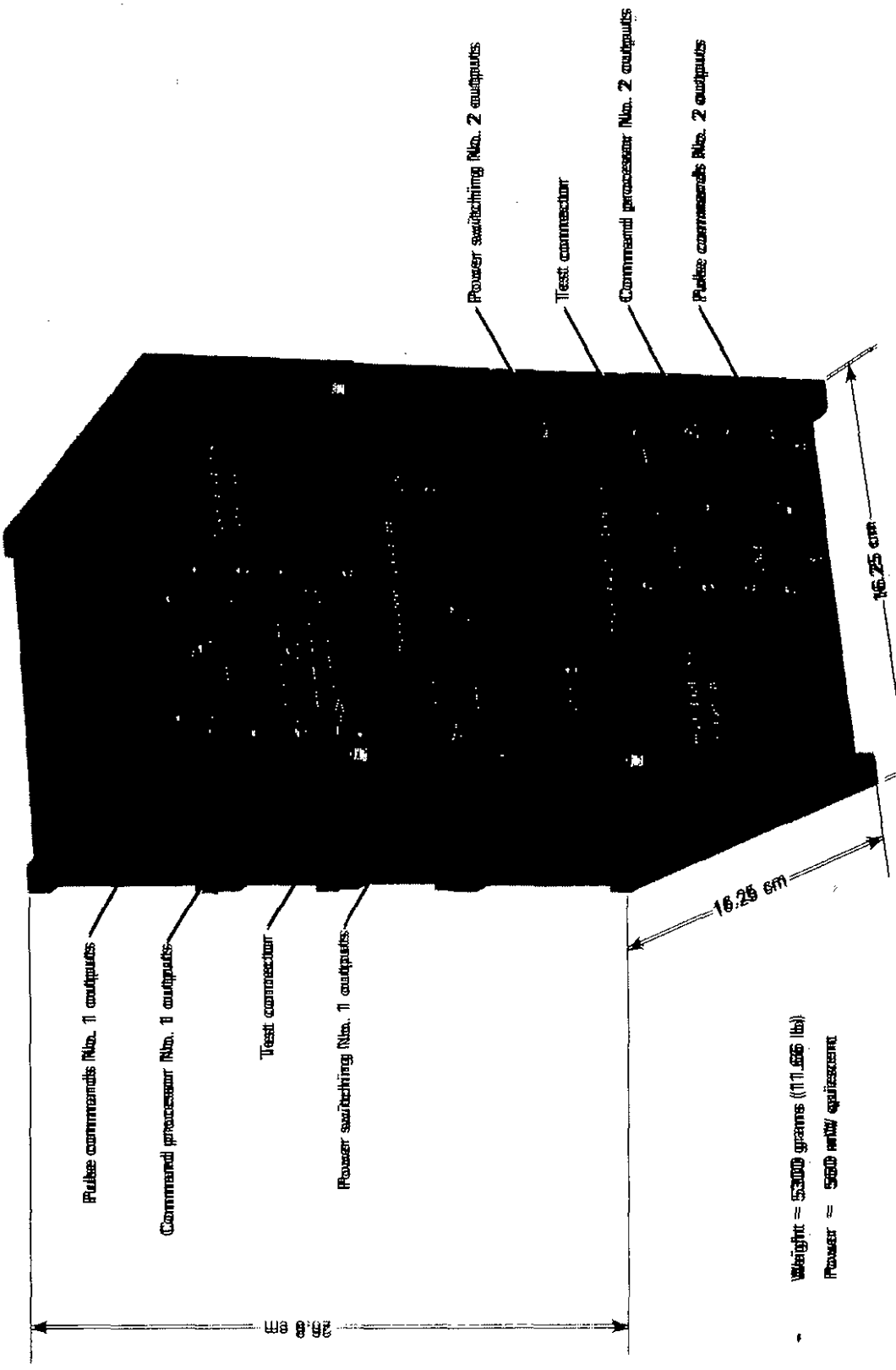

Fig. 6 MAGSAT command hardware.

HARDWARE

Approach. There are many guidelines and requirements associated with the design of spacecraft electronics that are, at best, very demanding and in some cases somewhat contradictory. On the one hand, the power, weight, and volume for an on-board system must be minimized; yet reliability, the prime consideration, requires that the spacecraft function normally under severe mechanical vibrations (during launch) and hostile environmental conditions (temperature, vacuum, and radiation) of outer space. In many instances the satellite must function for many years. Reliability considerations tend to add weight, power, and volume — because one method of improving reliability is to integrate redundant systems. Additionally, for many programs there is a requirement for hardware delivery on an ambitious schedule.

Redundancy. The reliance of all the on-board satellite systems on the command system for normal configuration and control, as well as for an abnormal troubleshooting tool, in conjunction with the telemetry system, contributes to the decision for redundancy. There are essentially two independent addressable channels, each consisting of a receiver, processor, and power-switching electronics. Both channels have equivalent command capabilities so that failure in any one channel would not impair any command function. In addition to channel redundancy, a measure of circuit redundancy exists within each channel. Circuit redundancy is integrated into the design to reduce further the probability of executing erroneous commands. To reinforce the redundancy, numerous software checks are made on the command message. These must be verified successfully or the processor will abruptly terminate the command message processing. (This will be further amplified in the software section.) It is better not to execute any commands than to execute a wrong command.

It is not possible to completely eliminate erroneous commands caused by random failures within each command processor. However, it is possible to limit erroneous commands by noting such an anomaly via the telemetered command telltales (one per command) and then selecting the other command channel for subsequent spacecraft operations. There is an address latch in each of the processors that must be set for the execution of all but the delayed commands load command. This address latch is under software control and is set only for successful satellite address, processor select bits, and

Hamming byte decoding. The setting of the address latch enables other software controlled signals to be generated for the execution of the desired command.

In addition to circuit redundancy, other precautions were taken in the generation of the set of signals required for each of the various command functions. Signal splitting early in the signal generation chain, with subsequent processing and independent buffering, provide some measure of protection from random component failures. For the case of the relay matrix commands, there are two sets of signals, a relay capacitor bank charge, and a set of relay select drive signals, which must occur simultaneously for relay commands. For data commands, there are four signals for each user: (a) select, (b) clock, (c) data, and (d) execute, which are distributed between separate interface circuits. Data command users are advised to use all four signals appropriately before acting on the transmitted data. Similar multiple enables constrain the execution of pulse commands.

Microprocessor Family. The CDP 1802 family of circuits, consisting of the CDP 1802 microprocessor, the CDP 1852 interface circuit, the CDP 1822 1 k x 1 RAM, and the HA 6611 256 x 4 PROMS are the core of this design. The RCA CDP 1802 is the LSI CMOS 8-bit register-oriented central-processing unit (CPU). The CDP 1802 contains all the circuitry for the fetching, interpreting, and execution of instructions stored in external memory and the generation of numerous I/O control signals. There is a 16-bit scratch-pad register array with individual registers designated by a 4-bit binary code for the register-controlled operations. Three of those registers are specified by the N, P, and X (4-bit) registers (Fig. 7). The N register is a designator required for certain CPU instructions. The P register selects a register to be the current program counter. The X designator selects one of the 16 registers as a pointer to memory for an operand for certain ALU and I/O operations. The CDP 1802 has a program interrupt mode, four I/O flags that can be directly tested by branch instructions, and an on-chip DMA capability.

The CDP 1802 is fabricated with static silicon-gate CMOS circuitry that eliminates requirements for dynamic memory refreshing. A 2-MHz single-phase clock was selected based on various systems' considerations, thus resulting in 8 μs instruction time for a majority of the 91 CPU instructions. All instructions are two 8-clock-pulse machine cycles with the exception of the long-branch statements, which require three machine cycles. The first

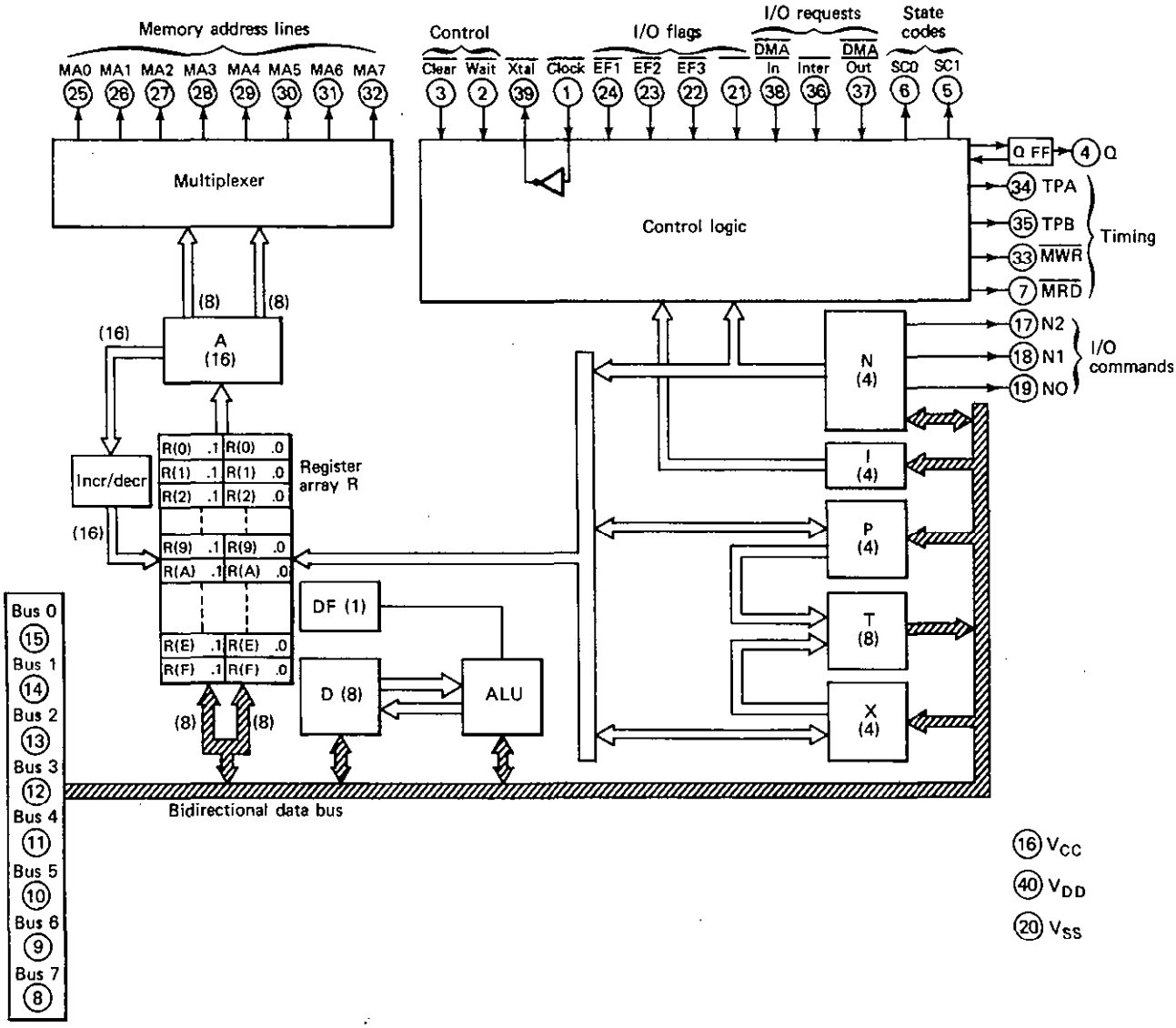

Fig. 7 Microstructure of the CDP 1802.

cycle performs the fetching; the second and third cycles perform the execution. Memory bytes are multiplexed during each machine cycle so that the CDP 1802 microprocessor can address 2^{16} bytes.

Board Electronics. Each command processor is composed of four electronics boards that are interconnected via flexible cabeling. The four boards fold in an accordian fashion and are housed in a magnesium casting 16 by 16 by 8 cm. Figure 8 shows the processor; Fig. 9 is the block diagram. Board 1 contains the CDP 1802 microprocessor, its clock, address decode, and latch circuitry. Eighteen of the 22 Harris CMOS 6611A PROMS and all the CMOS CDP 1822 RAM are on board 1. There are 2816 bytes of PROM that are organized as 11 sets of two 256 by 4 HA 6611A PROMS. There are 1024 bytes of RAM organized as eight 1024 x 1 CDP 1822 circuits. The RAMS are the dual in-line (DIP) packages seen in the lower left side of board 1. A 51-pin service connector on the rear of this board allows manual controls on the CPU and logic analyzer monitoring of the CPU program flow. This connector will be connected to a dummy mate in the flight configuration.

The ROM circuit (UT4) on board 1 contains the utility programs for CPU, program control, and diagnostics. Three functions are performed by this utility program: (a) questioning of the memory, (b) loading of programs to a specified area of RAM, and (c) start of programs loaded in memory. The program loading feature was used during the breadboard stage to load command programs that were assembled on the APL 360/370 computers to RAM for software development and verification. UT4 and associated supporting memory circuits were removed for the flight configuration. Figure 10 is a map of the memory space.

There are four basic functions performed by the electronics on board 2 (Fig. 9) The test-control circuitry interacts with manual controls via board 1 to control the CDP 1802 microprocessor for normal or diagnostic operations. The output decode and control electronics provide various basic software control signals used throughout boards 2, 3, and 4. Specifically, the output decode circuits provide the three data commands, telemetry interfaces, and the drive signals for relay matrix commands. There are two short data command (24-bits fixed length) users — the star camera and the scalar magnetometer systems. The long data command (768 bits) is used by the attitude processor. The telemetry interface provides for the readback verification of delayed command loads. Relay matrix drive signals interface with the power switching modules for the execution of relay commands. In addition, there is a time-out counter with its associated independent clock used for erroneous jumps in the software sequencing. A 16-s counter is reset at the beginning of

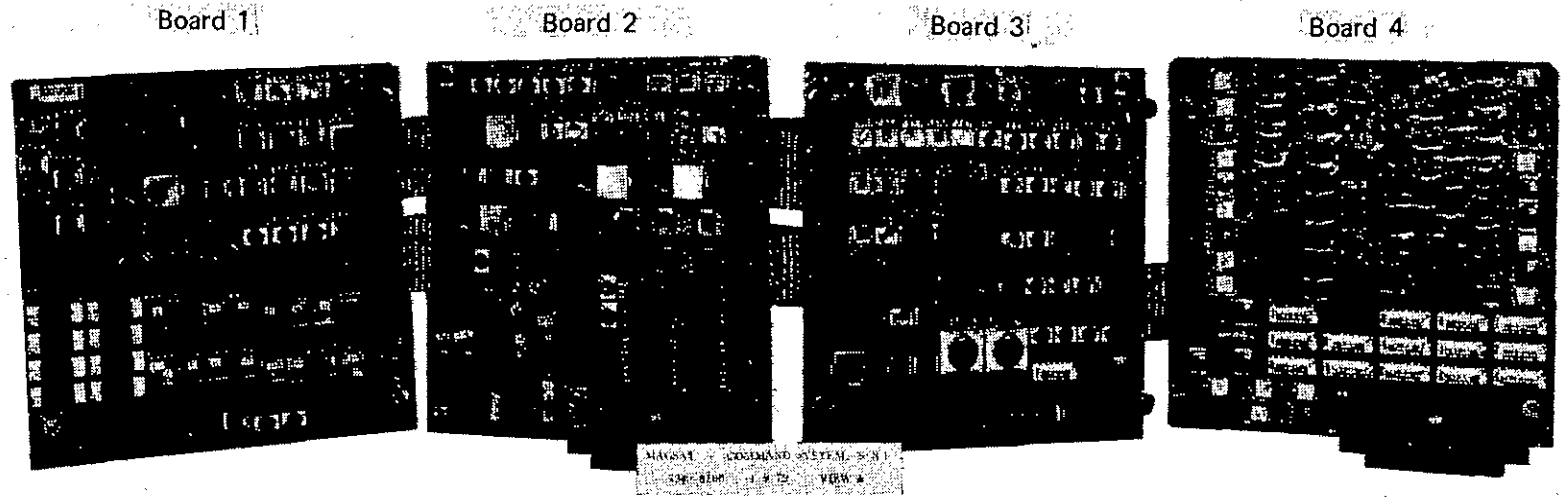

Fig. 8 Command processor hardware.

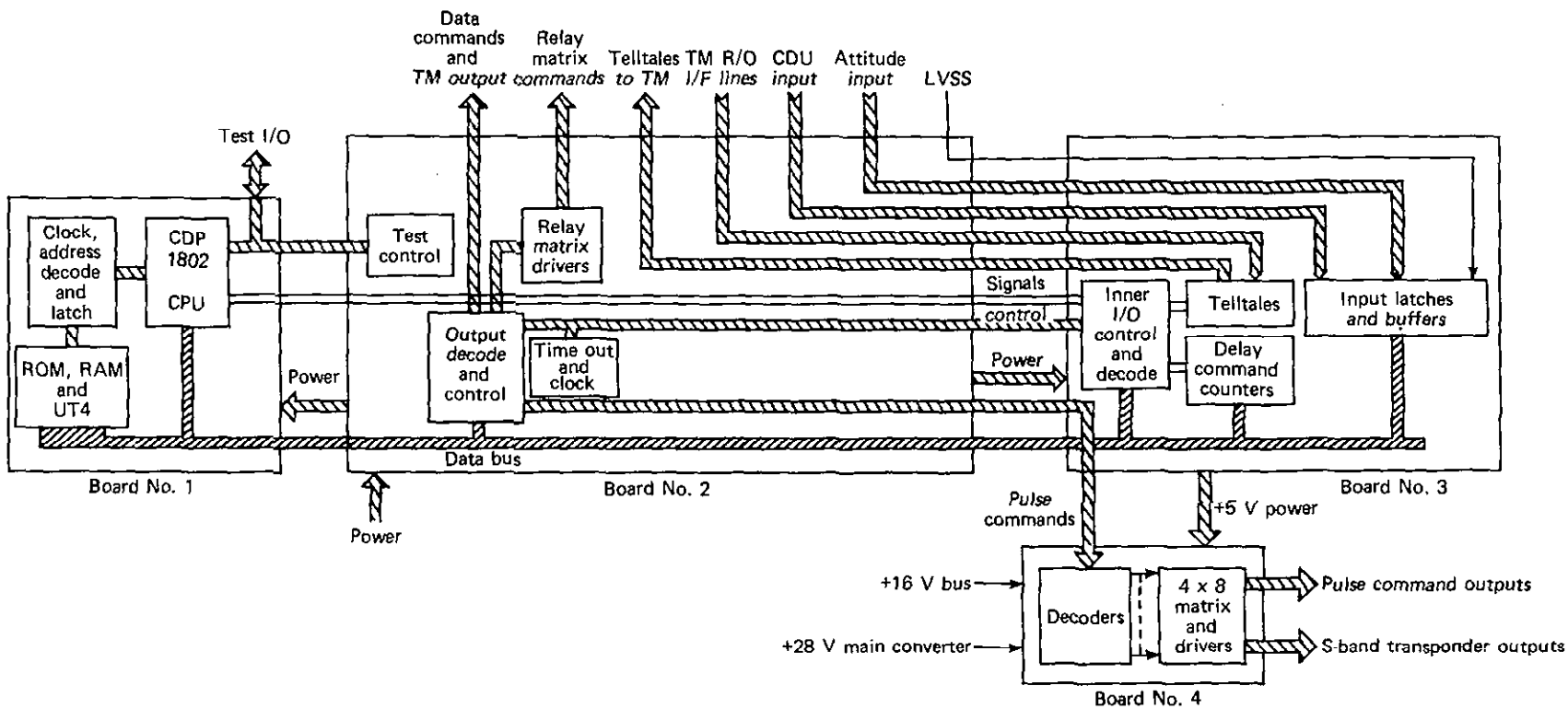

Fig. 9 Block diagram of MAGSAT command processor flight boards.

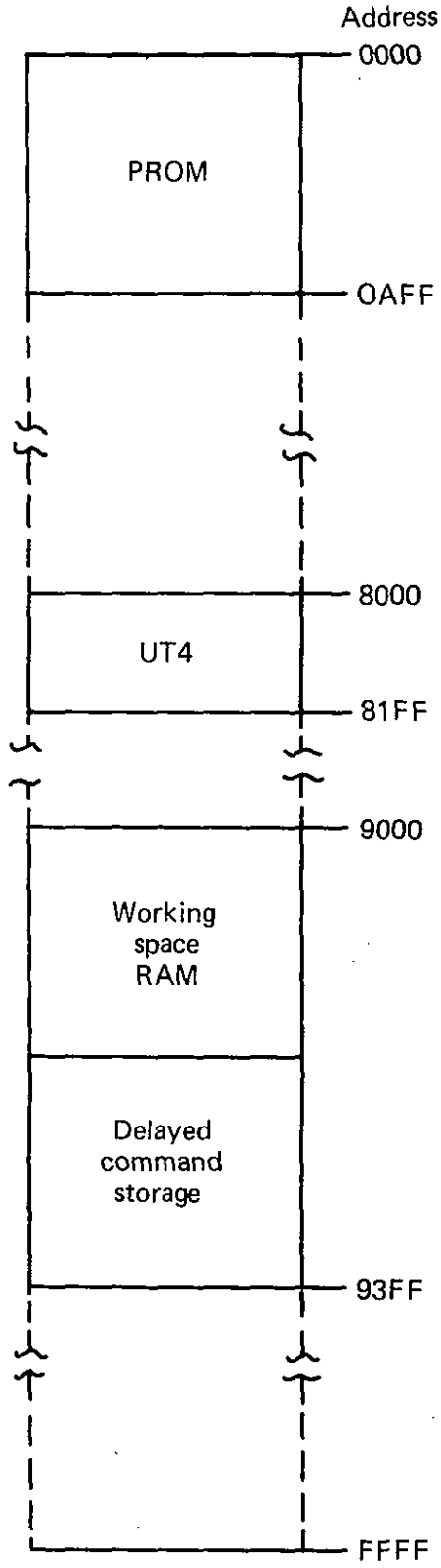

Fig. 10 Processor memory map.

the general polling (normal software sequencing) routine. If the counter is not reset because of anomalous conditions, a restart function is generated. The CDU interface signals route through board 2 to the electronics of board 3. Power inputs are via the 88-pin Hughes board 2 connector and are distributed to all four boards.

Board 3 contains the rest of the I/O control and decode circuitry. The various interrupts to the normal software flow are buffered and latched as may be seen in Fig. 9. Two delay command counters and their associated circuitry comprise a major function on board 3. Because of the 8-s least-significant bit timing for delayed commands, it is possible for the command system to process a cluster of delayed commands while the next command cluster is in que. With the two dedicated circuits and respective flags, delayed command timing integrity is preserved. Each command cluster can be potentially delayed 2^{14} x 8 s (36.4 h).

The last major function of board 3 is the four telltales that monitor the status of the command system. A real-time telltale indicates a "1" when real-time commands are being processed. A delayed-command telltale performs similarly. When high, the LVSS mask telltale indicates that the software controlled commands to be executed for low-voltage conditions is masked; that is, those commands will not be executed for LVSS interrupts. This was such a crucial situation as to warrant a specific telemetry telltale bit. Completing the telltale complement is the time-out bit. This bit is set to a "1" when the time-out counter (discussed as part of board 2) overflows and can only be reset via a hardware command. Such a command will perform selected signal setting or resetting functions internal to the command processor electronics.

Board 4 contains the electronics for the pulse command matrix. A 4 by 8 matrix can potentially switch 32 command functions in either a set or reset mode for distributed relay switching. Conceptually, the matrix provides source current to a user's relay in either direction to set or reset the relay contacts as shown in Fig. 11. When the pulse command is decoded, byte 7 information is routed to the decoding circuitry of the pulse-command matrix. Two additional pulse-command enables, one to switch power to the source/sink drivers and the other to enable the decoder outputs, serve to minimize erroneous outputs caused by random component failures. Once enabled, selected source sink drivers (PNP and NPN transistors) are switched on for 50 ms for the prescribed direction.

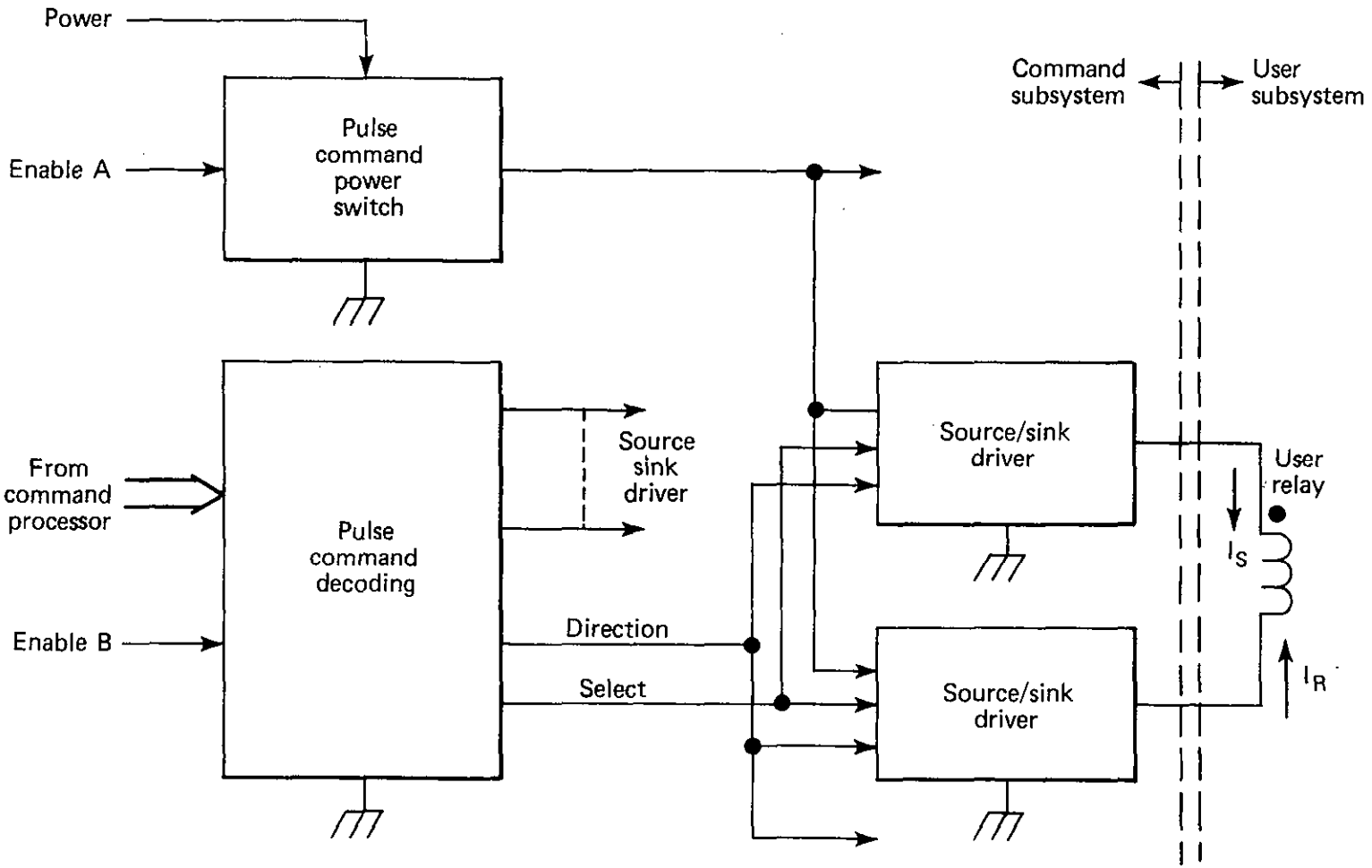

Fig. 11 Typical pulse command configuration.

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15. Supplementary Notes

16. Abstracts

A microprocessor-based command system has been designed, tested, fabricated, and flight qualified for integration into the MAGSAT spacecraft for the remote execution of relay, pulse, and data commands. Limited semiautonomous operations in conjunction with attitude, power, and telemetry systems are featured. A stored memory of 2.8 kilobytes in CMOS PROMS with 1 k bytes of random access CMOS memory provide the program and the working space for the microprocessor to decode command messages. The design represents the first in a new generation of command systems for satellites designed at APL and offers expanded user capabilities, increased flexibility in real time, and delayed command operations.

17. Key Words and Document Analysis. 17a. Descriptors

Spacecraft
flight control

Spacecraft control
attitude control
remote control

Spacecraft maneuvers
spacecraft control

Spacecraft communication
radio communication

Magnetic surveys
geomagnetism
magnetic anomalies

Magnetic fields
geomagnetism

17b. Identifiers/Open-Ended Terms

Earth's magnetic field
magnetic crustal anomalies

Microprocessor control circuits
spacecraft communications

Integrated circuits

17c. COSATI Field/Group 0814, 0905, 1702.1, 1706, 1707, 2201, 2202, 2203

18. Availability Statement	19. Security Class (This Report) UNCLASSIFIED	21. No. of Pages 38
	20. Security Class (This Page) UNCLASSIFIED	22. Price

The capability of selecting the direction of current flow through a user relay allows for an efficient relay utilization for redundancy. Dual coil, magnetically latching relays are required for pulse command users. Each coil of each pulse command relay is assigned to a pulse matrix for independent control of the relay contacts. The circuit redundancy ends at the internal electromechanical interface of the relay.

Power Switching. The power switching matrices interface with the relay command matrix signals generated on board 2 for centralized power and signal distribution. These matrices, which are fabricated with the cordwood technique, also use the principle of current steering through relay coils. The current pulse is generated by turning on selected SCRs in the 8 × 7 matrix to discharge a set of capacitors through the addressed relays. The capacitor bank is charged only for relay matrix commands.

The two relay matrices provide for operations using low voltage sensing switches (LVSS). When a low voltage is sensed, an LVSS circuit external to the command system will provide a pulse to switch off all nonessential satellite loads. The same pulse is also routed to each command processor to initiate LVSS stored commands actuation.

SOFTWARE

Approach. In a microprocessor design, the distribution between software and hardware is an important consideration. A large portion of signal processing can be performed via software controlled signal decoding and generation; however, a reliable design must not rely too heavily on any one technique. There must be a judicious mixture of hardware-software dependency. The philosophy of this distribution for the command system was to perform decoding for signal generation via firmware for the various unlocks, enables, and byte manipulations. Hardware decoding for relay pulse commands complement the circuit redundancy and signal splitting techniques previously discussed. In addition, the software performs various checks and balances on the command message itself before any command can be executed successfully. These checks were designed to reject command message corruption caused by inadvertent message generation or RF uplink noise.

Routines. Details of the firmware distribution are shown in Fig. 12. There are four basic routines: INGENPOL, CMDEX, INTRCDLD, and STORED CMDS. INGENPOL performs the processor initialization when the power is turned on, at restart, and for post LVSS operations. It also provides for the background mode for continually executing the general polling routine shown in Fig. 4. The outer loop of general polling depicts the various interrupts with priority beginning with the processing of real-time commands. The CMDEX routine is called to process command frames within each loop of the general polling routine. When a command is processed, the CMDEX routine returns the processor to INGENPOL. Real-time command sequences are loaded into each processor's RAM by interrupting INGENPOL with INTRCDLD. The STORED CMDS portion of the firmware consists of the commands that are executed via software for processing the various interrupt operations.

Eight flags or interrupts are interrogated by INGENPOL. All are maskable but the real-time processing loop. The real-time (R/T) flag is set when commands are loaded into each processor's RAM. When INGENPOL detects the R/T flag, the real-time command sequence is executed. Each processor detects its respective R/T flag, but only the addressed processor executes the real-time command sequence. Each command in the sequence is processed individually by calling CMDEX, with subsequent INGENPOL sampling of all flags of lower priority, before returning to the real-time loop to process another command. The last command in the real-time sequence resets the R/T flag and clears the RAM working space.

Because of the serious nature of low battery voltages, the second highest priority is assigned to power control operations. For the low-voltage conditions, the LVSS maskable flag is set via an external circuit. For the anomalous low-voltage conditions, seven stored commands located in each processor's STORED CMDS PROM space are executed in sequence. Each processor executes the same seven stored commands since both LVSS flags are set simultaneously. Both processors reinitialize before returning to the general polling looping.

There are two delayed commands flags serviced by INGENPOL. At time-out, all commands in a cluster are processed sequentially before INGENPOL returns to the outer loop to service other flags. Thus, the smallest time between delayed command clusters can be 4 s (each relay command requires 1.009 s as a minimum of 8 s is required between clusters).

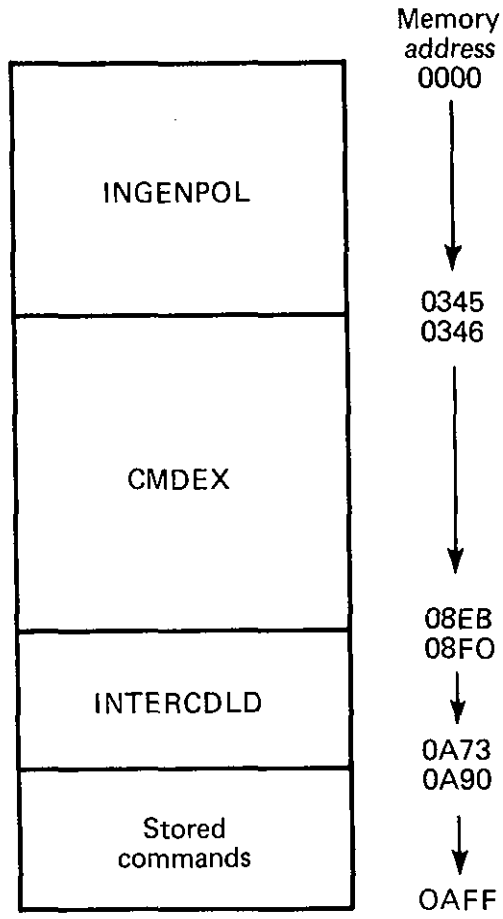


Fig. 12 MAGSAT command firmware.

The three attitude flags are next in priority. These flags serve to control the attitude of MAGSAT in conjunction with the onboard attitude processor by executing the following functions in a semiautonomous mode: (a) Z coil power, (b) spin system power, and (c) spin system sense direction. Interrupts from the nonredundant attitude processor are buffered separately and routed to both command processors. Selected lines from the attitude system sequence the same attitude maneuvers through both command processors in a redundant fashion.

Last in priority is the S-band turn-off function. Since the S-band transmitter places a heavy load on the MAGSAT power system, it is extremely important not to have the transmitter turned ON after a pass. Therefore a flag is set in INGENPOL to turn the transmitter OFF 12.5 min after a transmitter ON command.

In the processing of the various flags, INGENPOL keeps track of the sources of the commands to be executed. One of the 16-bit scratch registers of the CDP 1802, R8, is used as the command pointer linkage. For each interrupt (flag), INGENPOL extracts from RAM a dedicated pointer that defines the start of the eight command bytes to be processed for execution and passes it via register R8 to CMDEX.

INGENPOL also keeps track of the number of real-time commands, the number of delayed command clusters, and the number of commands left in the cluster. It also performs various range checks on these numbers.

CMDEX is a separate subroutine that occupies X'0346' to X'08EB' in PROM space. This program saves the INGENPOL CPU status in RAM, extracts and processes the eight command bytes for execution, and returns to the general polling routine. During the processing, CMDEX performs many checks on the command frame for proper coding before outputting the various desired command signals. Initially the Hamming byte is verified to check for link errors. The satellite processor-select bits are then checked for the selection of the processor in order to continue processing the remainder of the command frame. Up to this point any unsuccessful comparisons result in the abortion of the command. Additional paths occur to command abortion when other checks, such as undefined or illegal destination coding, are detected. Upon the successful processing of all the checks, CMDEX will generate signals for the execution of relay, pulse, short data, long load, and TM readout via software control functions.

INTRCDLD is the third separate routine in PROM space occupying X'08F0' to X'0A73'. This routine processes the command message as shown in Fig. 3. Both command processors acknowledge the CPU signals to interrupt its respective INGENPOL looping to potentially load in real-time command sequences. Many successful checks must again be verified before the real-time command frames are extracted from the data stream and loaded into the RAM working space for subsequent execution. INTRCDLD initially checks for a checkerboard pattern. The program detects data patterns that differ from the checkerboard and searches for the synchronization byte. Before a real-time command sequence is accepted, 16 contiguous checkerboard bits starting with a "1" must immediately preface the sync byte. If the previous conditions are not satisfied within a 256-bit data stream, then an immediate return to INGENPOL occurs; otherwise the ensuing command frames are loaded into the working RAM space. The time limit on this detection is designed to control the interrupt time. The loading of the command frames is controlled to a maximum of 256 bytes.

The stored CMDS portion of PROM, X'0A90' to X'0AFF', contains the command frames for the seven LVSS, six attitude, and one transponder OFF command required for the various loops in INGENPOL.

Software for this project was developed with the in-house APL-generated 1802 cross-assembler. The various subroutines were individually cross-assembled to produce object codes that were loaded into the command breadboard RAM with the UT4 utility program. Program revisions were almost on a real-time basis. At the completion of the program development, PROM's were programmed in conjunction with a Data I/O PROM Programmer.

FLIGHT QUALIFICATION

The command system uses 840 connector pins to communicate with the other systems onboard MAGSAT. Most of those connections are command outputs. Each output must be monitored for all commands to determine actual command performance. Only those output pins associated with a particular command should change for execution of that command. The check of all command outputs for the 4 data, 56 relay, and 32 pulse commands per processor on a manual basis is totally impractical. Consequently, an automated test configuration for the flight qualification of the command system was developed.

The following discussion assumes that all of the command processor boards have been individually debugged and successfully integrated with both of the power switching modules.

The automated testing is centered about a SEL 32 computer (Fig. 13). The computer is involved in the automated generation of commands by the command modulator and for interrogation and checking of a command test bit stream (14752 bits generated within the command system tester). The command test bit stream characterizes the output status of the entire command system. Every command function causes an individual response within an assigned portion of the data stream (Fig. 14). The three parts of this test bit stream are: (a) processor A, (b) processor B, and (c) pulse and relay command status. The processor A and B portions are equivalent. They monitor the data and the command load outputs. Individual RAM memories in the tester are loaded for each command data function and are multiplexed into the test data stream, which eventually is compared by the SEL 32 for proper bit changes. The pulse and relay power switching bits are composed of series shift registers that monitor the relay contact outputs.

An automated test sequence, consisting of a deck of input cards per processor, exercises each processor through an inclusive set of relay, data, pulse commands, and LVSS operations on both a real time and a delayed basis. The test-bit stream in the command tester and then a reference table in the SEL 32 are initialized by sending the appropriate commands. After each command is executed, the command tester is interrogated by the SEL 32 for the command results by shifting the entire test-bit stream into the SEL 32 memory. A set of cards changes the appropriate bits for that command in the SEL reference table. A comparison is made by the SEL on the updated reference table and the test-bit stream data. Successful comparison results in the continuation of the test sequence. An unsuccessful comparison halts the test. The line printer prints out the bit errors and displays the first few errors. A full test for the redundant command system at one temperature and at one voltage requires about four hours. For troubleshooting, manual intervention of this test sequence is possible via: (a) the video display keyboard, (b) the command modulator keyboard, or (c) individual testing command cards via the card reader.

Each processor has passed the tests listed in Table 2. In Table 2, "potting" refers to the conformal coating on the front and back of all electronics boards. The post-vibration qualification included exercising and testing the command system through three thermal cycles.

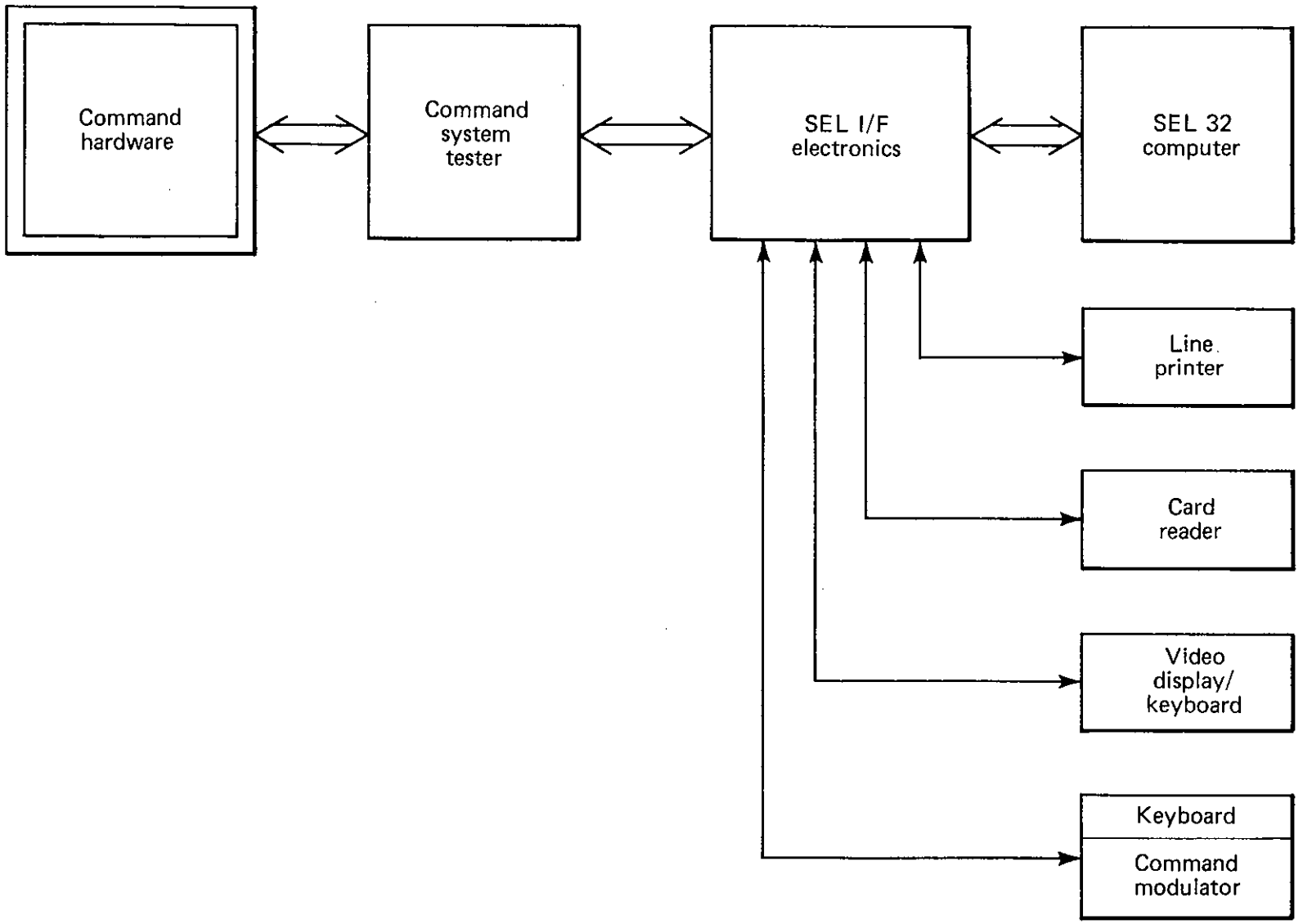
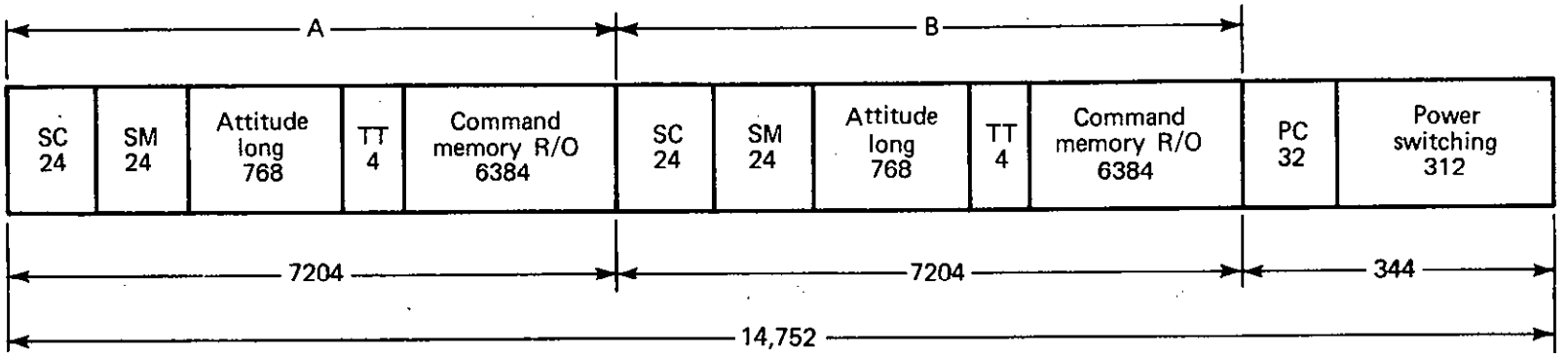


Fig. 13 Command system test configuration.



SC: Star camera
SM: Scalar magnetometer
PC: Pulse command
TT: Telltale

Fig. 14 MAGSAT command test bit stream structure.

Table 2

Command system testing cycle

Condition	Temperature (°C)	Voltage
Prepotting	+25	Nominal
	+60	High and Low
	-25	High and Low
Postpotting	+25	Nominal
Vibration	+25	Nominal
Postvibration	+25	Nominal
	+60	High and Low
	-25	High and Low

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