



The Control Console directs and monitors all activities of the Intellec 4. Complete processor status and machine cycle conditions are displayed, and operational control of all processor activity is provided. Additional controls facilitating program debugging and hardware checkout are included on the control console.

**ADDRESS** is a display of the current address being accessed in program memory.

**1.** INDICATORS 0-11 are a display of the memory address being displayed during CMA or SEARCH operations. (see CMA and SEARCH ADDRESS CONTROL, 18-24)

**STATUS** is a display of the operating mode of the processor.

2. SEARCH COMPLETE indicates the processor has executed instructions until the search address and pass counter settings have been reached. (see SEARCH ADDRESS CONTROLS, 17-21 and PASS COUNTER, 17)

**3.** CPU indicates the processor is operating.

**4.** POINTER VALID indicates that the LAST RAM/ROM POINTER is valid. (see LAST RAM/ROM POINTER 11)

**INSTRUCTION** is a display of the information contained in the currently addressed location in memory.

**5.** INDICATORS 0-3 (M2) and 4-7 (M1) are a display of the instruction fetched at M1 and M2 from the location displayed in ADDRESS. (see ADDRESS 1)

**ACTIVE BANK** is a display of the active bank of RAM data storage memory.

**6.** CM-RAM 0-3 indicators display the active bank of RAM selected on the previous DCL command.

**MODE** is a display of the active bank of program memory. (see MODE CONTROL 14, 15 and 16)

7. MON indicates the memory containing the Resident System Monitor is active.

**8.** PROM indicates that the PROM program memory bank is active.

**9.** RAM indicates the RAM program memory bank is active.

**EXECUTION** is a display of the processor data bus during execution of an instruction.

**10.** INDICATORS 0-7 display the contents of the processor bus during X2 and X3 execution times.

**LAST RAM/ROM** POINTER is a display of the current RAM and ROM address pointer.

**11.** INDICATORS 0-7 are a display of X2 and X3 during the last SRC (send register control) command. Validity of this display is indicated by the POINTER VALID display. (see POINTER VALID 4)

ADDRESS/DATA consists of twelve switches through which both memory addresses and data are entered during SEARCH and CMA operation. (see SEARCH ADDRESS 18-22 and CMA 25 & 26)

**12.** SWITCHES 0-11 are used to enter memory addresses for SEARCH MODE and CMA operation. (see SEARCH ADDRESS CONTROLS, 18-22 and CMA 23 and 24)

**13.** SWITCHES 0-7 are used to enter data into RAM PROGRAM MEMORY during a CMA operation. (see CMA 25 and 26)

**MODE CONTROL** consists of three switches which select the bank of program memory from which the processor executes code.

**14.** MON selects the bank of memory containing the system monitor.

**15.** RAM selects the RAM program memory bank for execution.

**16.** PROM selects the optional PROM program memory for execution.

## PASS COUNTER

**17.** SWITCHES 0-3 enter the data for successive passes through the search address during a SEARCH OPERATION.

## SEARCH ADDRESS CONTROLS:

These switches control SEARCH MODE and CMA addressing. (see CMA 25 and 26)

**18.** RUN overrides SEARCH MODE OPERATION.

**19.** NEXT INST. causes search mode to terminate at the next location following the designated search address.

**20.** DECR decrements the address loaded from the ADDRESS/DATA switches by one.

**21.** INCR increments the address loaded from the ADDRESS/DATA switches by one.

**22.** LOAD loads the address from the ADDRESS/DATA switches into an address register for SEARCH MODE or CMA operation.

## TEST

**23.** HOLD sets the processor TEST line to a true or false condition.

**24.** ONE SHOT momentarily pulses the processor TEST line to a true condition.

CMA Console Memory Access

**25.** Enables and disables the console memory access feature.

**26.** WRITE deposits the data in ADDRESS/DATA switches 0-7 in the memory address previously loaded from the ADDRESS/DATA switches.

## **RESET CONTROL**

**27.** RESET causes the processor or the system to be reset, depending upon the MODE 28.

**28.** MODE allows either the system or the CPU only to be reset.

## **POWER and PROM**

**29.** PROGRAM PROM POWER enables the high voltage for PROM programming.

**30.** PROGRAM PROM is a zero insertion force socket for the PROM to be programmed.

**31.** POWER is the master system power switch.

#### **Standard Systems and Optional**

**Modules:** Intellec 4 (imm 4-40A) Standard system includes the following modules and accessories:

- Central Processor Module
- Memory Control Module
- RAM Memory Module
- PROM Programmer Module
- Chassis with mother board
- Power Supplies
- Control and Display Console
- Finished Cabinet
  Standard Software System Monitor Assembler

# **Optional Modules and Accessories**

- □ I/O Modules
- Data Storage Modules
- Instruction/Data Storage Modules
- PROM Memory Module
- Universal Prototype Module
- □ Module Extender
- Rack Mounting Kit

