System Design Considerations When Using Cypress CMOS Circuits

This application note describes some factors to consider when either designing new systems using Cypress high-performance CMOS integrated circuits or when using Cypress products to replace bipolar or NMOS circuits in existing systems. The two major areas of concern are device input sensitivity and transmission line effects due to impedance mismatching between the source and load.

To achieve maximum performance when using Cypress CMOS ICs, pay attention to the placement of the components on the printed circuit board (PCB); the routing of the metal traces that interconnect the components; the layout and decoupling of the power distribution system on the PCB; and perhaps most important of all, the impedance matching of some traces between the source and the loads. The latter traces must, under certain conditions, be analyzed as transmission lines. The most critical traces are those of clocks, write strobes on SRAMs and FIFOs, output enables, and chip enables.

Replacing Bipolar or NMOS ICs

Cypress CMOS ICs are designed to replace both bipolar ICs and NMOS products and to achieve equal or better performance at one-third (or less) the power of the components they replace.

When high-performance Cypress CMOS circuits replace either bipolar or NMOS circuits in existing sockets, be aware of conditions in the existing system that could cause the Cypress ICs to behave in unexpected ways. These conditions fall into two general categories: device input sensitivity and sensitivity to reflected voltages.

Input Sensitivity

High-performance products, by definition, require less energy at their inputs to change state than low- or medium-performance products.

Unlike a bipolar transistor, which is a current-sensing device, a MOS transistor is a voltage-sensing device. In fact, a MOS circuit design parameter called K′ is analogous to the gm of a vacuum tube and is inversely proportional to the gate oxide thickness.

Thin gate oxides, which are required to achieve the desired performance, result in highly sensitive inputs. These inputs require very little energy at or above the device input-voltage threshold (approximately 1.5V at 25°C) to be detected. CMOS products may detect high-frequency signals to which bipolar devices may not respond.

MOS transistors also have extremely high input impedances (5 to 10 MΩ), which make the transistors' gate inputs analogous to the input of a high-gain amplifier or an RF antenna. In contrast, because bipolar ICs have input impedances of 1000Ω or less, these devices require much more energy to change state than do MOS ICs. In fact, a typical Cypress IC requires less than 10 picojoules of energy to change state. Thus, when Cypress CMOS ICs replace bipolar or NMOS ICs in existing systems, the CMOS ICs might respond to pulses of energy in the system that are not detected by the bipolar or NMOS products.

Reflected Voltages

Cypress CMOS ICs have very high input impedances and—to achieve TTL compatibility and drive capacitive loads—low output impedances. The impedance mismatch due to low-impedance outputs driving high-impedance inputs might cause unwanted voltage reflections and ringing under certain conditions. This behavior could result in less-than-optimum system operation.

When the impedance mismatch is very large, a nearly equal and opposite negative pulse reflects back from the load to the source when the line's electrical length (PCB trace) is greater than

$$l = \frac{t_r}{2t_{pd}} \qquad \text{Eq. 1}$$

where t_r is the rise time of the signal at the source, and t_{pd} is the one-way propagation delay of the line per unit length.

The classical way of stating the condition for a voltage reflection to occur is that it will occur if the signal rise time is less than or equal to the round-trip (two-way) propagation delay of the line.

Input clamping diodes to ground were added to bipolar IC families (e.g., TTL, AS, LS, ALS, FAST) when the circuit designers decided that the fast rise and fall times of the outputs could cause voltage reflections. The clamping diodes to V_{CC} are inherent in the junction isolation process. For a more detailed explanation, see "Input/Output Characteristics of Cypress Products."

Historically, as circuit performance improved, the output rise and fall times of the bipolar circuits decreased to the point where voltage reflections began to occur (even for short traces) when an impedance mismatch existed between the line and the load. Most users, however, were unaware of these reflections because they were suppressed by the diodes' clamping action.

Conventional CMOS processing results in PN junction diodes, which adversely affect the ESD (electrostatic discharge) protection circuitry at each input pin and cause an increased susceptibility to latch-up. In addition, when the input pin is negative enough to forward bias the input clamping diodes, electrons are injected into the substrate. When a sufficient number of electrons are injected, the resulting current can disturb internal nodes, causing soft errors at the system level.

To eliminate the prospect of having this problem, all Cypress CMOS products use a substrate bias generator. The substrate is maintained at a negative 3V potential, so the substrate diodes cannot be forward biased unless the voltage at the input pin becomes a diode drop more negative than –3V. (See *Figure 9* in "Input/Output Characteristics of Cypress Products" for a schematic of the input protection circuit used in all Cypress CMOS products.) To the systems designer, this translates to approximately five times (3.8V divided by 0.8V =4.75) the negative undershoot safety margin for Cypress CMOS integrated circuits versus those that do not use a bias generator.

Voltage reflections should be eliminated by using impedance matching techniques and passive components that dissipate excess energy before it can cause soft errors. Crosstalk should be reduced to acceptable levels by careful PCB layout and attention to details.

Crosstalk

The rise and fall times of the waveforms generated by Cypress CMOS circuit outputs are 2 to 4 ns between levels of 0.4 and 4V. The fast transition times and the large voltage swings could cause capacitive and inductive coupling (crosstalk) between signals if insufficient attention is paid to PCB layout.

Crosstalk is reduced by avoiding running PCB traces parallel to each other. If this is not possible, run ground traces between signal traces.

In synchronous systems, the worst time for the crosstalk to occur is during the clock edge that samples the data. In most systems it is sufficient to isolate the clock, chip select, output enable, and write and read control lines from each other and from data and address lines so that the signals do not cause coupling to each other or to the data lines.

It is standard practice to use ground or power planes between signal layers on multilayered PCBs to reduce crosstalk. The capacitance of these isolation planes increases the propagation delay of the signals on the signal layers, but this drawback is more than compensated for by the isolation the planes provide.

The Theory of Transmission Lines

A connection (trace) on a PCB should be considered as a transmission line if the wavelength of the applied frequency is short compared to the line length. If the wavelength of the applied frequency is long compared to the length of the line, conventional circuit analysis can be used.

In practice, transmission lines on PCBs are designed to be as nearly lossless as possible. This simplifies the mathematics required for their analysis, compared to a lossy (resistive) line.

Ideally, all signals between ICs travel over constant-impedance transmission lines that are terminated in their characteristic impedances at the load. In practice, this ideal situation is seldom achieved for a variety of reasons.

Perhaps the most basic reason is that the characteristic impedances of all real transmission lines are not constants, but present different impedances depending upon the frequency of the applied signal. For "classical" transmission lines driven by a single frequency signal source, the characteristic impedance is "more constant" than when the transmission line is driven by a square wave or a pulse.

According to Fourier series expansion, a square wave consists of an infinite set of discrete frequency components-the fundamental plus odd harmonics of decreasing amplitude. When the square wave propagates down a transmission line, the higher frequencies are attenuated more than the lower frequencies. Due to dispersion, the different frequencies do not travel at the same speed.

Dispersion indicates the dependence of phase velocity upon the applied frequency (see Reference 1, page 192). The result is that the square wave or pulse is distorted when the frequency components are added together at the load.

A second reason why practical transmission lines are not ideal is that they frequently have multiple loads. The loads may be distributed along the line at regular or irregular intervals or lumped together, as close as practical, at the end of the line. The signal-line reflections and ringing caused by impedance mismatches, non-uniform transmission line impedances, inductive leads, and non-ideal resistors could compromise the dynamic system noise margins and cause inadvertent switching.

One system design objective is to analyze the critical signal paths and design the interconnections such that adequate system noise margins are maintained. There will always be signal overshoot and undershoot. The objective is to accurately predict these effects, determine acceptable limits, and keep the undershoot and overshoot within the limits.

The Ideal Transmission Line

An equivalent circuit for a transmission line appears in *Figure 1*. The circuit consists of subsections of series resistance (R) and inductance (L) and parallel capacitance (C) and shunt admittance (G) or parallel resistance, R_p. For clarity and consistency, these parameters are defined per unit length. Multiply the values of R, L, C, and R_p by the length of the subsection, *l*, to find the total value. The line is assumed to be infinitely long.

If the line of *Figure 1* is assumed to be lossless (R = 0, R_p = infinity), *Figure 1* reduces to *Figure 2*. A small series resistance has little effect upon the line's characteristic impedance. In practice and by design, the series resistance is quite small. For 1-ounce (0.0015-inch-thick), 1-mil-wide (0.010-inch) copper traces on G-10 glass epoxy PCBs, the trace resistance is between 0.5 and 0.3Ω per foot. 2-ounce copper has a resistance 50 percent lower than that of 1-ounce copper.

Input or Characteristic Impedance

To calculate the characteristic impedance (also called AC impedance or surge impedance) looking into terminals a-b of the circuit in *Figure 2*, use the following procedure.

Let Z_1 be the input impedance looking into terminals a-b, with Z_2 for terminals c-d, Z_3 for terminals e-f, etc. Z_1 is the series impedance of the first inductor (*l*L) in series with the parallel combination of Z_2 and the impedance of the capacitor (*l*C).

From AC theory:

$$X_L = j\omega lC \qquad \text{Eq. 2}$$

where X_L is the inductive reactance.

$$X_C + \frac{1}{j\omega lC} \qquad \text{Eq. 3}$$

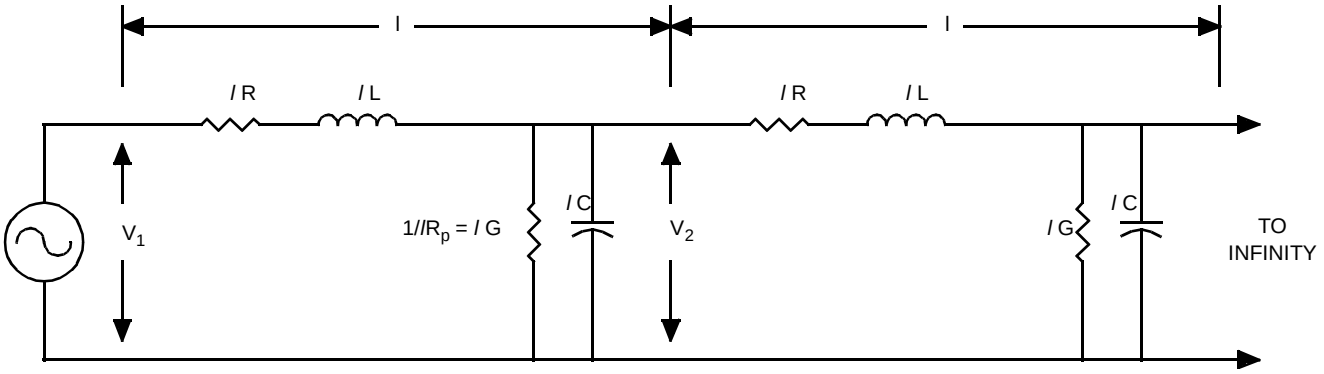


Figure 1. Transmission Line Model

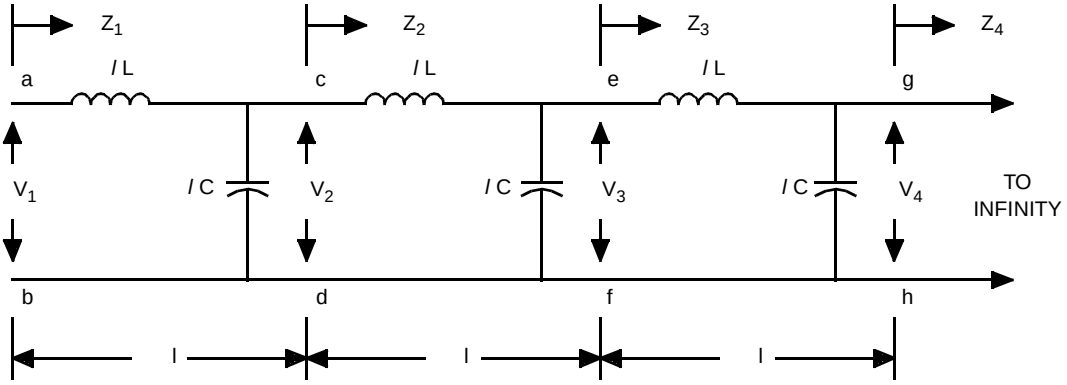


Figure 2. Ideal Transmission Line Model

where X_C is the capacitive reactance.

Then

$$Z_1 = X_L + \frac{Z_2 X_C}{Z_2 + X_C} \quad \text{Eq. 4}$$

If the line is reasonably long, $Z_1 = Z_2 = Z_3$. Substituting $Z_1 = Z_2$ into *Equation 4* yields

$$Z_1 = X_L + \frac{Z_1 X_C}{Z_1 + X_C}$$

or

$$Z_1^2 - Z_1 X_L - X_C X_L = 0 \quad \text{Eq. 5}$$

Substituting the expressions for X_C and X_L yields

$$Z_1^2 - j\omega l L = \frac{L}{C} \quad \text{Eq. 6}$$

Equation 6 contains a complex component that is frequency dependent. The complex component can be eliminated by allowing *l* to become very small and by recognizing that the ratio L/C is constant and independent of *l* or ω:

$$Z_1 = \sqrt{L/C} \quad \text{Eq. 7}$$

The AC input impedance of a purely reactive, uniform, lossless line is a resistance. This is true for AC or DC excitation.

Propagation Velocity and Delay

The propagation velocity (or phase velocity) of a sinusoid traveling on an ideal line (see Reference 1) is

$$\alpha = \frac{1}{\sqrt{LC}} \quad \text{Eq. 8}$$

The propagation delay for a lossless line is the reciprocal of the propagation velocity:

$$t_{pd} = \sqrt{LC} = Z_1 C \quad \text{Eq. 9}$$

where L and C are once again the intrinsic line inductance and capacitance per unit length.

Adding additional stubs or loads to the line (see Reference 2 of this application note) increases the propagation delay by the factor

$$\sqrt{1 + C_D/C} \quad \text{Eq. 10}$$

where C_D is the load capacitance.

Therefore, the propagation delay of a loaded line, T_{pdL}, is

$$t_{pdL} = t_{pd}\sqrt{1 + C_D/C} \quad \text{Eq. 11}$$

This application note shows later that a transmission line's unloaded or intrinsic propagation delay is proportional to the square root of the dielectric constant of the medium surrounding or adjacent to the line. Propagation delay is not a function of the line's geometry.

The characteristic impedance of a capacitively loaded line decreases by the same factor that the propagation delay increases:

$$Z_1' = \frac{Z_1}{\sqrt{1 + C_D/C}} \quad \text{Eq. 12}$$

Note that the capacitance per unit length must be multiplied by the line length, *l*, to calculate an equivalent lumped capacitance.

The Condition for Voltage Reflection

It is relatively straightforward to obtain a closed-form solution for a transmission line's maximum allowable length, which, if exceeded, might cause a voltage reflection. If the line is not terminated in its characteristic impedance, a reflection is guaranteed to occur. The reflection's amplitude depends on the amount of impedance mismatch between the line and the load and whether the rise time of the signal at the source equals or is greater (slower) than two times the propagation delay of the line.

The condition for a voltage reflection to occur is

$$L \geq \frac{t_r}{2t_{pdL}} \quad \text{Eq. 13}$$

Solving for the loaded propagation delay yields

$$t_{pdL} = \frac{t_r}{2L} \quad \text{Eq. 14}$$

However, the actual physical length of the line is

$$l = \frac{t_r}{t_{pd}} \quad \text{Eq. 15}$$

The intrinsic capacitance of the line from *Equation 9* is

$$C_O = \frac{T_{pd}}{Z_O} \quad \text{Eq. 16}$$

It is standard practice to use C_O to designate the intrinsic line capacitance, L_O the intrinsic line self inductance, and Z_O the intrinsic line characteristic impedance.

Substituting *Equations 14*, *15*, and *16* into *Equation 11* gives the relationship for the line length at which voltage reflections might occur. Two conditions must be present for voltage reflections to occur: the line must be long and there must be an impedance mismatch between the line and the load.

$$\frac{t_r}{2L} = t_{pd}\sqrt{1 + \frac{C_D}{\frac{t_r}{t_{pd}} \times \frac{t_{pd}}{Z_O}}} \quad \text{Eq. 17}$$

Solving *Equation 17* for the line length, L, yields

$$L = \frac{t_r}{2t_{pd}} \times \frac{1}{\sqrt{1 + \frac{C_D Z_O}{t_r}}} \quad \text{Eq. 18}$$

Equation 18 is very useful to the system designer. It is generic and applies to all products irrespective of circuit type, logic family, or voltage levels. The equation allows you to estimate when a line requires termination, using variables you can easily determine.

When driving a distributed or non-lumped load, the signal's rise time depends on the source—not the load, as you might expect. The intrinsic, or unloaded, line propagation delay per unit length is a function of the dielectric constant and can be easily calculated. The intrinsic line characteristic impedance is a function of the dielectric constant and the PCB's physical construction or geometry and can also be calculated. Finally, you can estimate the equivalent (lumped) load capacitance by adding up the number of loads (device inputs) being driven and multiplying by 10 pF. For I/O pins, use 15 pF per pin.

Signal Transition Times

The standard Cypress 0.8µ (L drawn) CMOS process yields output buffers whose signals transition approximately 4V in 2 ns, or, have a slew rate of 2V per nanosecond. The rise time/fall time is 2 ns. Products fabricated using the Cypress BiCMOS process have the same rise times.

The Cypress ECL process yields products with 500-ps output signal rise times and fall times, or slew rates of 1V/0.5 ns = 2V per nanosecond. Internal signal slew rates are 10V per nanosecond, but only for short (usually less than 500 mV) voltage excursions. Thus, high-frequency noise is generated on chip, which you can eliminate by using 100- to 500-pF ceramic or mica filter capacitors between V_{CC} and ground.

The values in *Table 1* come from using *Equation 18* to calculate the line length at which voltage reflections may occur. The calculations assume a 50Ω intrinsic line characteristic impedance and that the PCB is multilayer, using stripline construction on G-10 glass epoxy material (dielectric constant of 5). These conditions result in an unloaded line propagation delay of 2.27 ns per foot.

Table 1. Line Length at Which a Voltage Reflection Occurs

t_r (ns)	C_D (pF)	L (inches)
2	10	4.73
2	20	4.32
2	40	3.74
2	80	3.05
1	10	2.16
1	20	1.87
1	40	1.53
1	80	1.18
0.5	10	0.93
0.5	20	0.76
0.5	40	0.59
0.5	80	0.44

Table 1 reveals that decreasing the source rise time from 2 to 0.5 ns (a factor of 4) decreases the line length at which a voltage reflection might occur by a factor of 5 (4.73 divided by 0.93 = 5.09) for the same load (10 pF) and intrinsic propagation delay (2.27 ns/ft.). A second observation is that for signals with rise times of 0.5 ns, all lines should be terminated.

Reflection Coefficients

Another attribute of the ideal transmission line, reflection coefficients, are not actually line characteristics. The line is treated as a circuit component, and reflection coefficients are defined that measure the impedance mismatches between the line and its source and the line and its load. The reason for defining and presenting the reflection coefficients becomes apparent later when it is shown that if the impedance mismatch is sufficiently large, either a negative or positive voltage might reflect back from the load to the source, and the voltage might either add to or subtract from the original signal. A mismatch between the source and line impedance may also cause a voltage reflection, which in turn reflects back to the load. Therefore, two reflection coefficients are defined.

For classical transmission lines driven by a single frequency source, the impedance mismatches cause standing waves. When pulses are transmitted and the source's output impedance changes depending upon whether a LOW-to-HIGH or a HIGH-to-LOW transition occurs, the analysis is complicated further.

You can use classical transmission line analysis-where pulses are represented by complex variables with exponentials-to calculate the voltages at the source and the load after several back and forth reflections. However, these complex equations tend to obscure what is physically happening.

Energy Considerations

Now consider the effects of driving the ideal transmission line with digital pulses and analyze the behavior of the line under various driving and loading conditions. The first task is to define the load and source reflection coefficients.

Figure 3 shows the circuit to be analyzed. The ideal transmission line of length *l* is driven by a digital source of internal resistance R_S and loaded with a resistive load R_L. The characteristic impedance of the line appears as a pure resistance,

$$(Z_O = \sqrt{L/C}) \qquad \text{Eq. 19}$$

to any excitation.

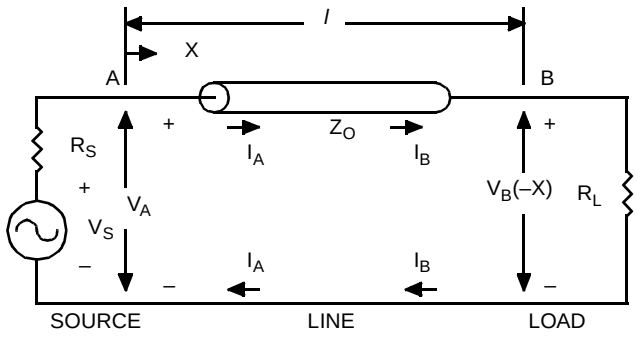


Figure 3. Ideal Transmission Line Loaded and Driven

The ideal case is when $R_S = Z_O = R_L$. The maximum energy transfer from source to load occurs under this condition, and no reflections occur. Half the energy is dissipated in the source resistance, R_S, and the other half is dissipated in the load resistance, R_L (the line is lossless).

If the load resistor is larger than the line's characteristic impedance, extra energy is available at the load and is reflected back to the source. This is called the underdamped condition, because the load under-uses the energy available. If the load resistor is smaller than the line impedance, the load attempts to dissipate more energy than is available. Because this is not possible, a reflection occurs that signals the source to send more energy. This is called the overdamped condition. Both the underdamped and overdamped cases cause negative traveling waves, which cause standing waves if the excitation is sinusoidal. The condition $Z_O = R_L$ is called critically damped.

The safest termination condition, from a systems design viewpoint, is the slightly overdamped condition, because no energy is reflected back to the source.

Line Voltage for a Step Function

To determine the line voltage for a step function excitation, you apply a step function to the ideal line and analyze the behavior of the line under various loading conditions. The step function response is important because any pulse can be represented by the superposition of a positive step function and a negative step function, delayed in time with respect to each other. By proper superposition, you can predict the response of any line and load to any width pulse. The principle of superposition applies to all linear systems.

According to theory, the rise time of the signal driven by the source is not affected by the characteristics of the line. This has been substantiated in practice by using a special coaxially constructed reed relay that delivers a pulse of 18A into 50Ω with a rise time of 0.070 ns (see Reference 1).

The equation representing the voltage waveform going down the line (see *Figure 3*) as a function of distance and time is

$$V_L(X,t) = V_A(t)U(t - Xt_{pd}) \text{ for } t < T_O \qquad \text{Eq. 20}$$

$$V_A(t) = V_S(t)\left(\frac{Z_O}{Z_O + R_S}\right) \qquad \text{Eq. 21}$$

where

V_A = the voltage at point A

X = the voltage at a point X on the line

l = the total line length

t_{pd} = the propagation delay of the line in nanoseconds per foot

$T_O = l\ t_{pd}$, or the one-way line propagation delay

U(t) = a unit step function occurring at x = 0

$V_S(t)$ = the source voltage

When the incident voltage reaches the end of the line, a reflected voltage, V′, occurs if R_L does not equal Z_O. The reflection coefficient at the load, ρL, can be obtained by applying Ohm's Law.

The voltage at the load is $V_L + V_L'$, which must be equal to $(I_L + I_L')R_L$. But

$$I_L = \frac{V_L}{Z_O} \quad \text{Eq. 22}$$

and

$$I_L' = -\frac{V_L'}{Z_O} \quad \text{Eq. 23}$$

(The minus sign is due to I_L being negative; i.e., I_L is opposite to the current due to V_L.) Therefore,

$$V_B = V_L + V_L' = \left(\frac{V_L}{V_O} - \frac{V_L'}{Z_O}\right)R_L \quad \text{Eq. 24}$$

By definition:

$$\rho_L = \frac{\textit{reflected voltage}}{\textit{incident voltage}} = \frac{V_L'}{V_L} \quad \text{Eq. 25}$$

Solving for V_L'/V_L in *Equation 24* and substituting in the equation for ρ_L yields

$$\rho_L = \frac{R_L - Z_O}{R_L + Z_O} \quad \text{Eq. 26}$$

The reflection coefficient at the source is

$$\rho_S = \frac{R_S - Z_O}{R_S + Z_O} \quad \text{Eq. 27}$$

Re-arranging *Equation 24* yields

$$V_B = V_L + V_L' = \left(1 + \frac{V_L'}{V_L}\right)V_L = (1 + \rho_L)V_L \quad \text{Eq. 28}$$

Equation 28 describes the voltage at the load (V_B) as the sum of an incident voltage (V_L) and a reflected voltage (ρ_L V*l*) at time t = T_O. When $R_L = Z_O$, no voltage is reflected. When $R_L < Z_O$, the reflection coefficient at the load is negative; thus, the reflected voltage subtracts from the incident voltage, giving the load voltage. When $R_L > Z_O$, the reflection coefficient is positive; thus, the reflected voltage adds to the incident voltage, again giving the load voltage.

Note that the reflected voltage at the load has been defined as positive when traveling toward the source. This means that the corresponding current is negative, subtracting from the current driven by the source.

This piecewise analysis is cumbersome and can be tedious. However, it does provide an insight into what is physically happening and demonstrates that a complex problem can be solved by dividing it into a series of simpler problems. Also, eliminating the exponentials—which provide phase information in the classical transmission line equations—simplifies the mathematics. To use the piecewise method, you must do careful bookkeeping to combine the reflections at the proper time. This is quite straightforward, because a pulse travels with a constant velocity along an ideal or low-loss line, and the time delay between reflected pulses can be predicted.

The rules to keep in mind are that at any location and time the voltage or the current is the algebraic sum of the waves traveling in both directions. For example, two voltage waves of the same polarity and equal amplitudes, traveling in opposite directions, at a given location and time add together to yield a voltage of twice the amplitude of one wave. The same reasoning applies to all points of termination and discontinuities on the line. The total voltage or current is the algebraic sum of all the incident and reflected waves. Polarities must be observed. A positive voltage reflection results in a negative current reflection and vice versa.

Step Function Response of the Ideal Line

Before examining reflections at the source due to mismatches between the source and line impedances, consider the behavior of the ideal line with various loads when driven by a step function. The circuit for analysis appears in *Figure 3*. *Figure 4* shows the voltage and current waveforms at point A (line input) and point B (the load) for various loads. (These values are drawn from Reference 1, pg. 158–159.) Note that $R_S = Z_O$ and that V_A at t = 0 equals $V_S/2$. This means that no impedance mismatch exists between the source and the line; thus, there is no reflection from the source at t = 2 T_O. T_O is the one-way propagation delay of the line.

The time-domain response of the reactive loads are obtained by applying a step function to the LaPlace transform of the load and then taking the inverse transform.

Note that the reflection coefficient at the load is not the total reflection coefficient (a complex number) but represents only the real part of the load. The piecewise method eliminates the complex ($j\omega t$) terms by performing the bookkeeping involving the phase relationships, which the complex terms account for in classical transmission line analysis.

Note that for the open-circuit condition in *Figure 4b*, Z_L = infinity, so that $\rho_L = +1$. The voltage is reflected from the load to the source (at amplitude $V_O = V_S/2$). Thus, at time t = 2 T_O, the reflected voltage adds to the original voltage, $V_O = V_S/2$, to give a value of $2V_O = V_S$. While the voltage wave is traveling down to and back from the load, a current of

$$I_O = \frac{V_O}{Z_O} = \frac{V_S}{2}Z_O \quad \text{Eq. 29}$$

exists. This current charges up the distributed line capacitance to the value V_S, then the current stops.

The waveforms at the source and load for the series RC termination shown in *Figure 4g* are of particular interest because this network dissipates no DC power; you can use this network to terminate a transmission line in its characteristic impedance at the input to a Cypress IC. *Figure 4h* represents the equivalent circuit of a Cypress IC's input. Combining both networks models a Cypress IC driven by a transmission line terminated in the line's characteristic impedance, when the values of R and C are properly chosen.

Reflections Due to Discontinuities

Figure 5 illustrates three types of common discontinuities found on transmission lines. Any change in the characteristic impedance of the line due to construction, connectors, loads, etc., causes a discontinuity, which causes a reflection that directs some energy back to the source. The amount of energy reflected back is determined by the discontinuity's reflection coefficient. Because discontinuities are usually small by design, most of the energy is transmitted to the load.

In general, a discontinuity has series inductance, shunt capacitance, and series resistance. An example is a via from a

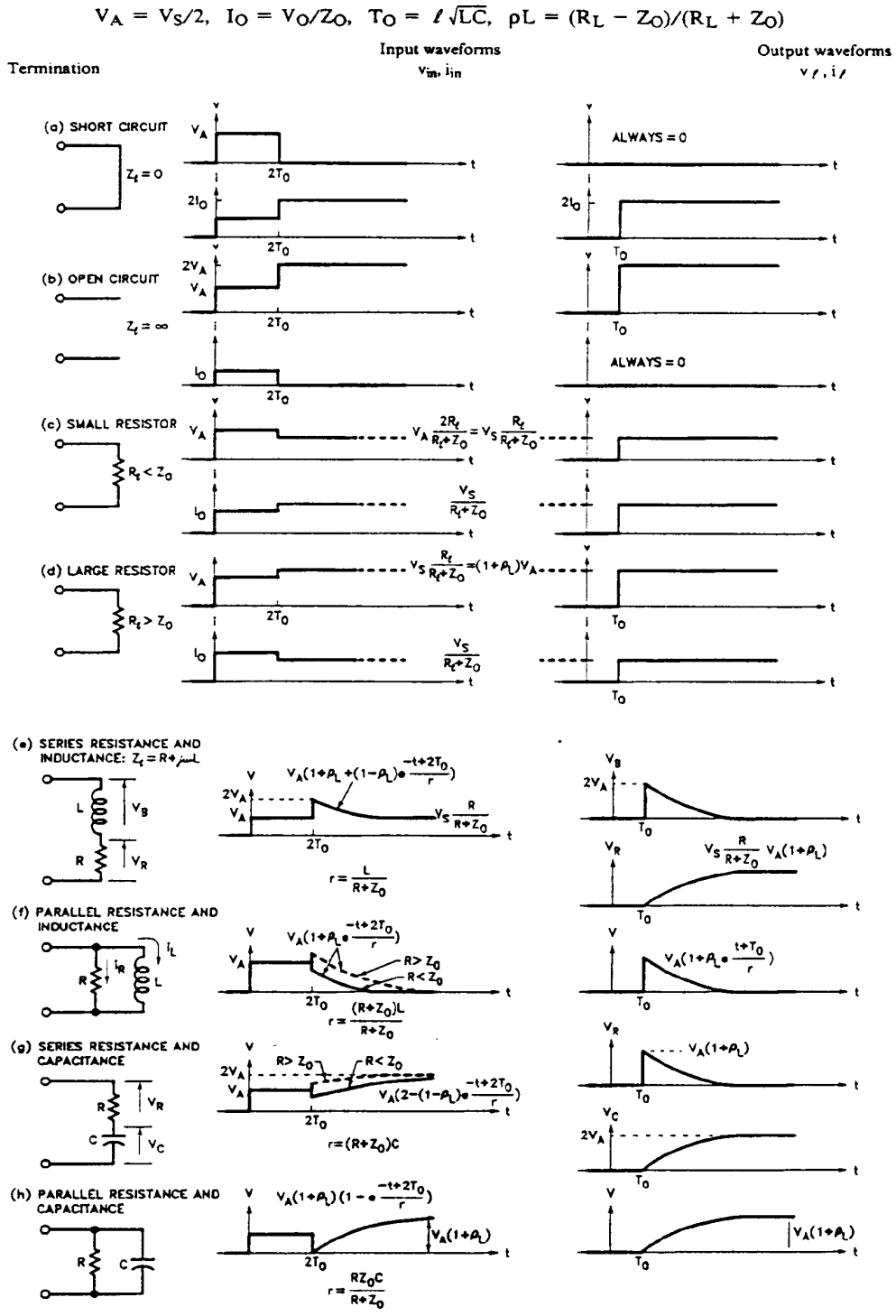


Figure 4. Step Function Response of *Figure 3* for Various Terminations

signal plane through a ground plane to a second signal plane in a multilayer PCB or module. IC sockets and other connectors can also cause discontinuities.

The Ideal Transmission Line's Pulse Response

Consider next the behavior of the ideal transmission line when driven by a pulse whose width is short compared to the

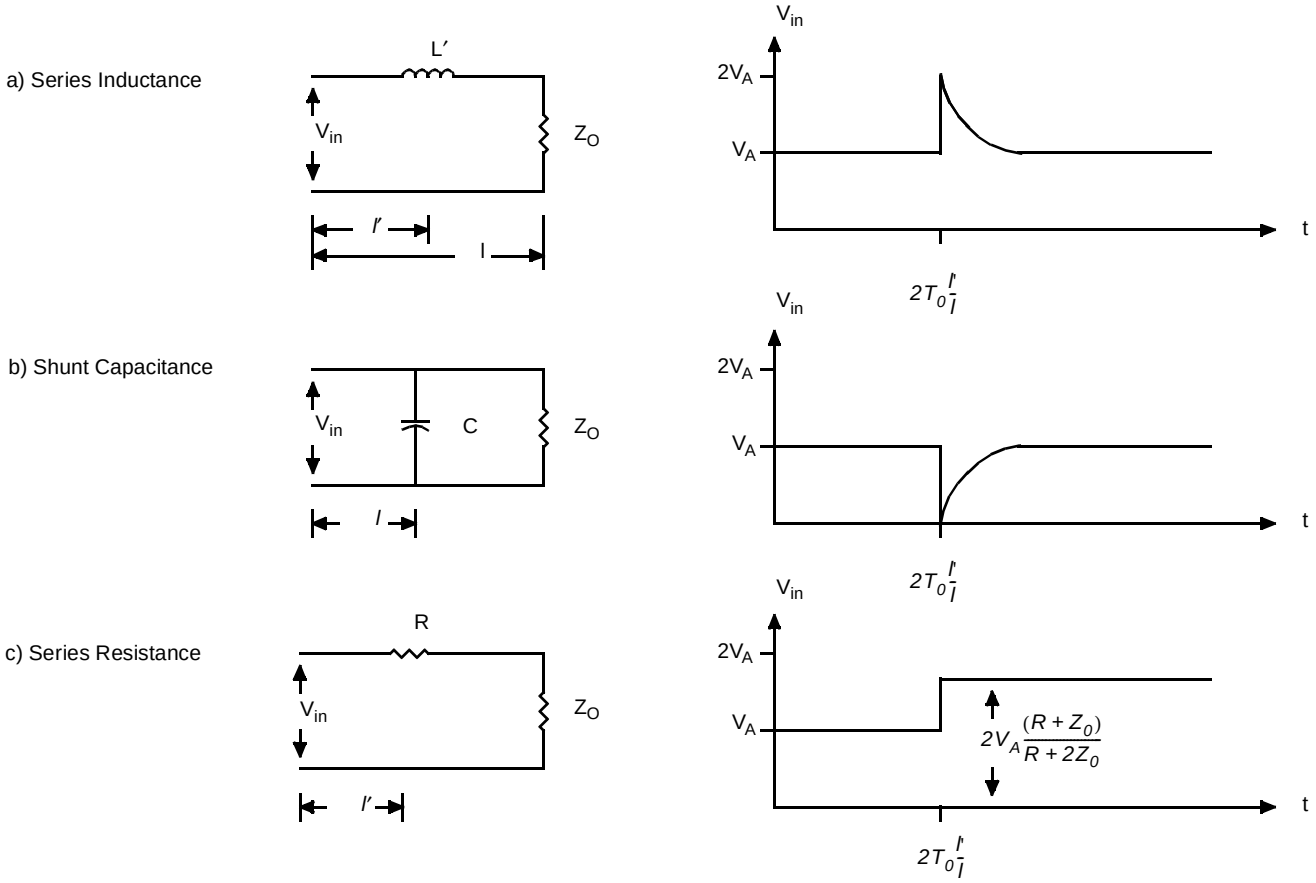


Figure 5. Reflections from Discontinuities with an Applied Step Function

line's electrical length-when the pulse width is less than the line's one-way propagation delay time, T_O.

Figure 6 shows another series of response waveforms for the circuit in *Figure 3*, this time for a pulse instead of a step (drawn from Reference 1, pg. 160–161). Note that $R_S = Z_O$ and that V_A at t = 0 equals $V_S/2$. This means that there is no impedance mismatch between the source and the line; thus, there is no reflection from the source at t = 2 T_O.

Finite Rise Time Effects

Now consider the effects of step functions with finite rise times driving the ideal transmission line. During the rise time of a pulse, half the energy in the static electric field is converted into a traveling magnetic field and half remains as a static electric field to charge the line.

If the rise time is sufficiently short, the voltage at the load changes in discrete steps. The amplitude of the steps depends on the impedance mismatch, and the width of the steps depends on the line's two-way propagation delay.

As the rise time and/or the line gets shorter (smaller T_O), the result converges to the familiar RC time constant, where C is the static capacitance. All devices should be treated as transmission lines for transient analysis when an ideal step function is applied. However, as the rise time becomes longer and/or the traces shorter, the transmission line analysis reduces to conventional AC circuit analysis.

Reflections from Small Discontinuities

Figure 7 shows a pulse with a linear rise time and rounded edges driving the transmission line of *Figure 5a* and *Figure 5b*. The expressions for V_r are derived on pages 171 and 172 of Reference 1. The reflection caused by the small series inductance is useful for calculating the value of the inductor, L′, but little else.

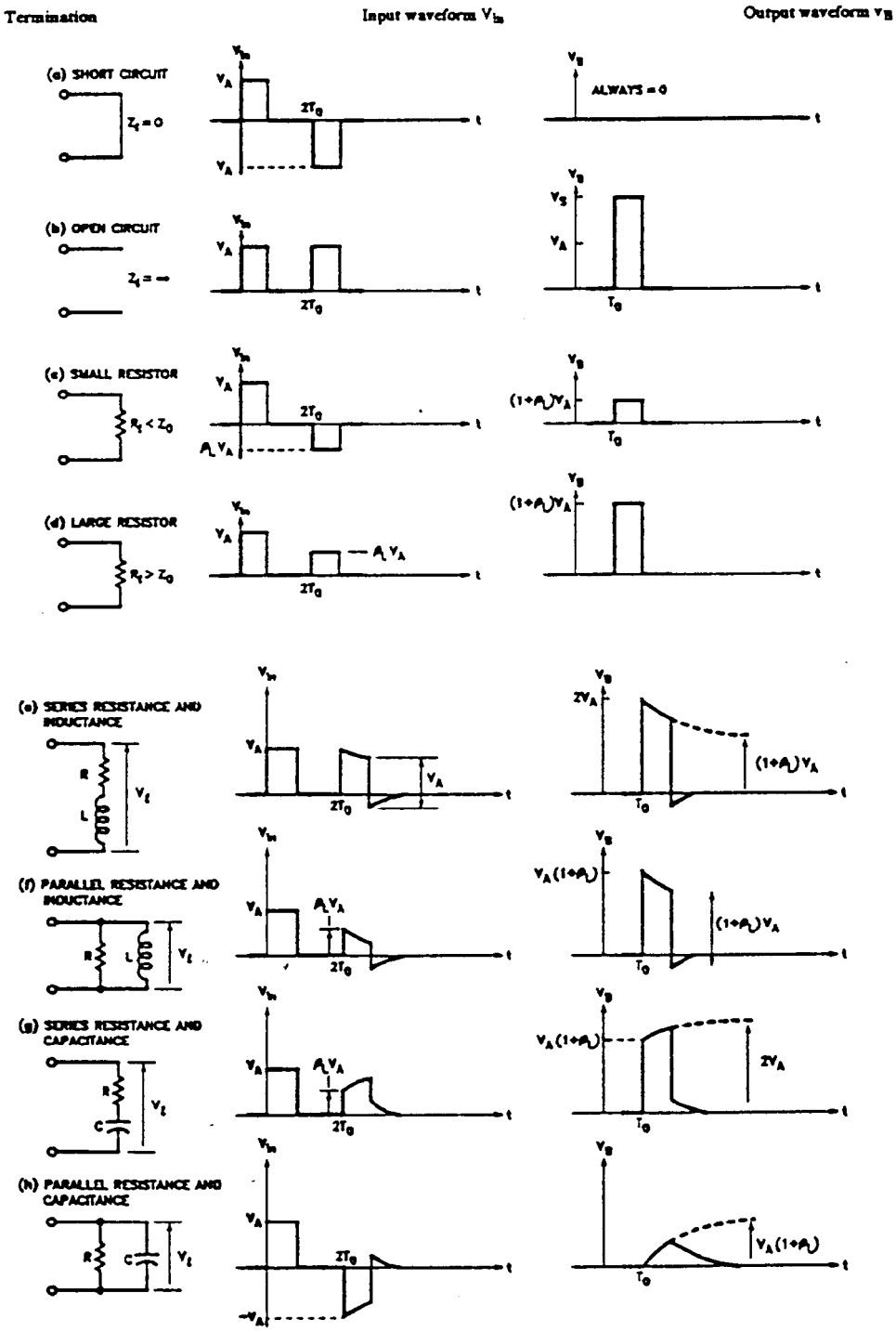
The reflection caused by the small shunt capacitor is more interesting. If this capacitor is sufficiently large, it can cause a device connected to the transmission line to see a logic 0 instead of a logic 1.

The Effect of Rise Time on Waveforms

Next, consider the ideal line terminated in a resistance less than its characteristic impedance and driven by a step function with a linear rise time. The stimulus, the circuit, and the response appear in *Figure 8a*, *Figure 8b*, and *Figure 8c*, respectively. Once again, note that because the source resistance equals the line characteristic impedance, there are no reflections from the source.

The resulting waveforms are similar to those of *Figure 4c* when modified as shown in *Figure 8c*. The final value of the waveform must be the same as before

The resultant wave at the line input (V_{in}) is easily obtained by superposition of the applied wave and the reflected wave at



$$V_A = V_S/2, \quad I_O = V_O/Z_o, \quad T_o = l\sqrt{LC}, \quad \rho_L = \frac{(R_L - Z_o)}{(R_L + Z_o)}$$

Figure 6. Pulse Response of *Figure 3* for Various Terminations

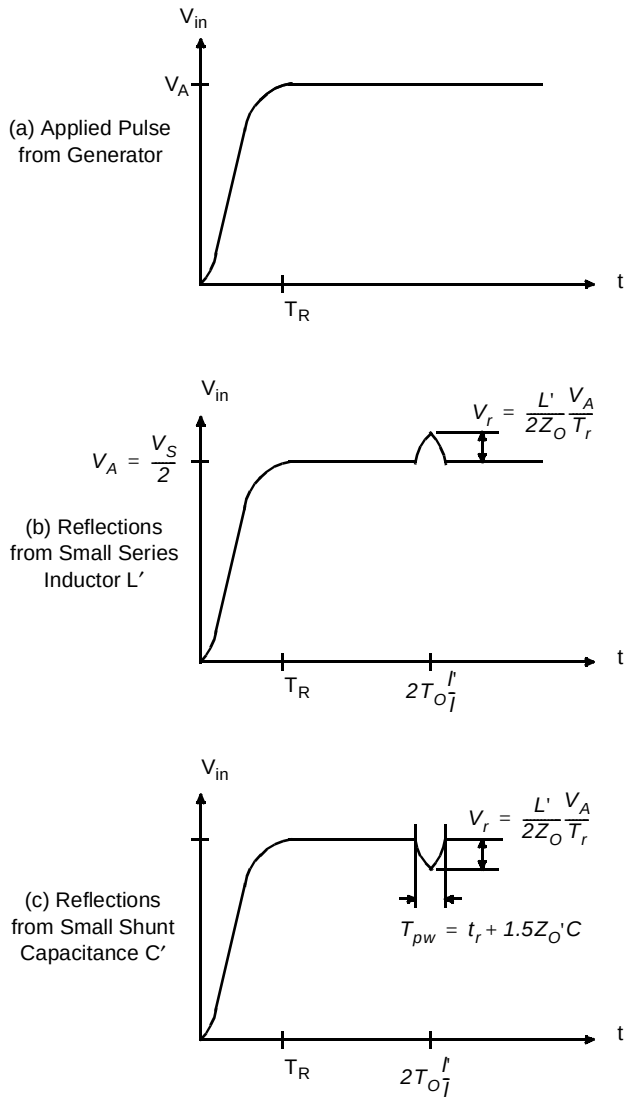


Figure 7. Reflections from Small Discontinuities with a Finite Rise Time Pulse

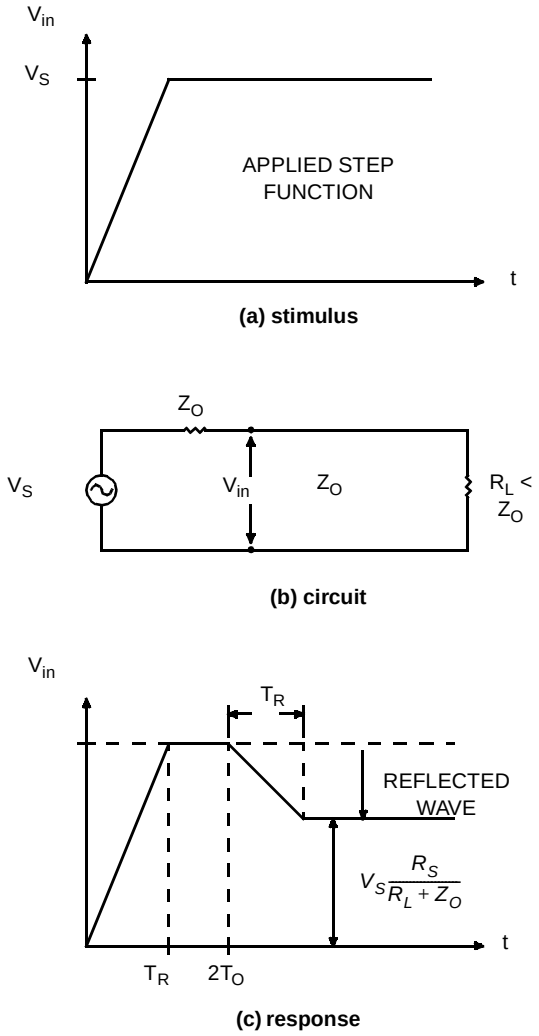


Figure 8. Effect of Rise Time on Response of Mismatched Line with $R_L < Z_O$

the proper time. In *Figure 8*, because the step function's rise time is less than the line's two-way propagation delay, the input wave reaches its final value, $V_S/2$. At t = 2 T_O, the reflected wave arrives back at the source and subtracts from the applied step function (the load reflection coefficient is negative). *Figure 9* illustrates waveforms for two relationships between the step function rise time and the propagation delay.

Multiple Reflections

Now consider the case of an ideal transmission line with multiple reflections caused by improper terminations at both ends of the line. The circuit and waveforms appear in *Figure 10*. The reflection coefficients at the source and the load are both negative-the source resistance and the load resistance are both less than the line characteristic impedance.

When the switch is initially closed, a step function of amplitude

$$V_O = V_{in} = \frac{V_S Z_O}{R_S + Z_O} \quad \text{Eq. 30}$$

appears on the line and travels toward the load. After a one-way propagation delay time, T_O, the wave reflects back with an amplitude of $\rho_L V_O$.

This first reflected wave then travels back to the source, and at time t = 2 T_O, the wave reaches the input end of the line. At this time, the first reflection at the source occurs, and a wave of amplitude $\rho_S (\rho_L V_O)$ reflects back to the load. At time t = 3 T_O, this wave again reflects from the load back to the source with amplitude

$$\rho_L \rho_S (\rho_L V_O) = \rho_S \rho_L^2 V_O \quad \text{Eq. 31}$$

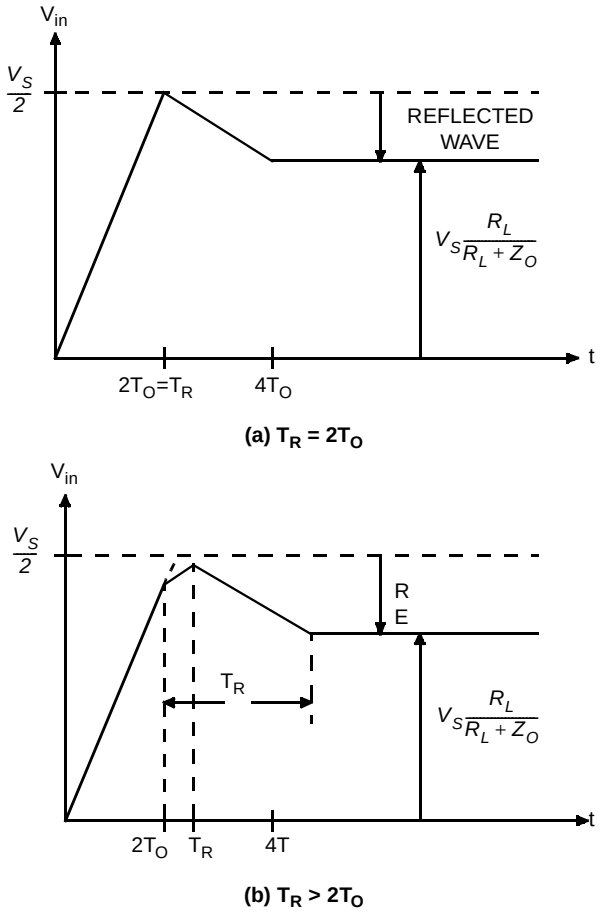


Figure 9. Effects of Rise Time on Response for $R_L < Z_O$

This back and forth reflection process continues until the amplitudes of the reflections become so small that they cannot be observed. The circuit is then said to be in a quiescent state.

Effective Time Constant

Voltage reflections in small increments and of short durations approximate an exponential function, as indicated by the dashed line in *Figure 10b*. The smaller and narrower the steps become, the more closely the waveform approaches an exponential curve.

The mathematical derivation is presented in Reference 1. The time constant is

$$K = -\frac{2T_O}{1-\rho_S\rho_L} \qquad \text{Eq. 32}$$

Thus, the resultant voltage waveform at the load can be approximated by

$$V(t) = V_O e\left(\frac{t}{K}\right) \qquad \text{Eq. 33}$$

For *Equation 32* to be accurate, ρ_L and ρ_S must be reasonably large (approaching ±1) so that the incremental steps are small. Because the product $\rho_S\rho_L$ is a positive number, less

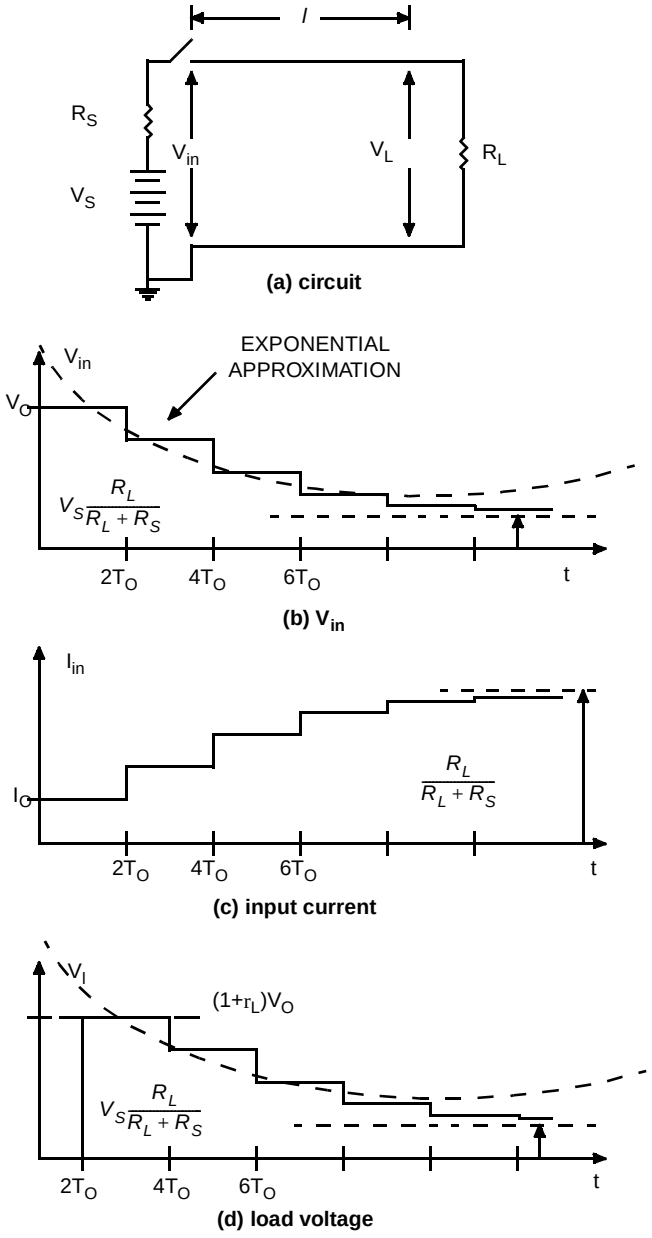


Figure 10. Step Function Applied to Line Mismatched on Both Ends; Shown for Negative Values of ρ_S and ρ_L

than one, the time constant is a negative number, which indicates that the exponential decreases with time. This is usually the case in transient circuits.

Both reflection coefficients must also have the same sign to yield a continually decreasing or increasing waveform. Opposite signs give oscillatory behavior that cannot be represented by an exponential function.

From Transmission Line to Circuit Analysis

When a transmission line is terminated in its characteristic impedance, the line behaves like a resistor. It usually does not

matter if you use transmission line or circuit analysis, provided that you take the propagation delays into account.

Consider the case of a short-circuited transmission line driven by a step function with a source impedance unequal to the characteristic line impedance. The general case is shown in *10a*. For $R_L = 0$ the reflection coefficients are

$$\rho_S = \frac{Z_S - Z_O}{Z_S + Z_O}, \rho_L = -1 \quad \text{Eq. 34}$$

The approximate time constant is

$$-k = \frac{2T_O}{1 - \rho_S\rho_L} = \frac{2T_O}{1 + \rho_S} = \frac{T_O(Z_S + Z_O)}{Z_S}$$

or

$$-k = T_O + \frac{T_O Z_O}{Z_S} \quad \text{Eq. 35}$$

Recall that

$$T_O = l\sqrt{LC} \quad \text{Eq. 36}$$

(one-way delay) and

$$Z_O = \sqrt{L/C} \quad \text{Eq. 37}$$

where *l* is the physical length of the line, and L and C are the per-unit-length parameters. Substituting these variables into *Equation 35* yields

$$-k = T_O = l\frac{L}{Z_S} \quad \text{Eq. 38}$$

It is necessary to have Z_S smaller than Z_O. Thus, the reflection coefficients have the same sign to give exponential behavior. Opposite signs give oscillatory behavior.

If $Z_S < Z_O$, the exponential approximation becomes more accurate. If Z_S is very small compared to Z_O, then T_O is negligible compared to lL/Z_O, so that *Equation 35* reduces to

$$k = -l\frac{L}{Z_S} \quad \text{Eq. 39}$$

But *l*L is the total loop inductance, and Z_S is the circuit's total series impedance. The time constant is then

$$k = \frac{L'}{R_S} \quad \text{Eq. 40}$$

This is the same time constant you would obtain by a circuit analysis approach if you considered the line a series combination of L′ and R_S. By open-circuiting the line and performing a similar analysis, it can be shown that an RC time constant results.

Types of Transmission Lines

The types of transmission lines include

- Coaxial cable
- Twisted pair
- Wire over ground
- Microstrip lines
- Strip lines

Coaxial Cable

Coaxial cable offers many advantages for distributing high-frequency signals. The well-defined and uniform characteristic impedance permits easy matching. The cable's ground shield reduces crosstalk, and the low attenuation at high frequencies make the cable ideal for transmitting the fast rise-time and fall-time signals generated by Cypress CMOS ICs. However, because of high cost, coaxial cable is usually restricted to applications that permit no alternatives. These applications usually involve clock distribution systems on PCBs or backplanes.

Because coaxial cable is not easily handled by automated assembly techniques, its application requires human assemblers. This requirement further increases costs.

Coaxial cables have characteristic impedances of 50Ω, 75Ω, 93Ω, or 150Ω. These values are the most common, although special cables can be made with other impedances.

Coaxial cable's propagation delay is very low. You can compute it using the formula

$$t_{pd} = 1.017\sqrt{e_r}(ns/ft) \quad \text{Eq. 41}$$

where e_r is the relative dielectric constant and depends upon the dielectric material used. For solid Teflon and polyethylene, the dielectric constant is 2.3. The propagation delay is 1.54 ns per foot. For maximum propagation velocity, you can use coaxial cables with dielectric Styrofoam or polystyrene beads in air. Many of these cables have high-characteristic impedances and are slowed considerably when capacitively loaded.

Twisted Pair

You can make twisted pairs from standard wire (AWG 24–28), twisted about 30 turns per foot. The typical characteristic impedance is 110Ω.

Because the propagation delay is directly proportional to the characteristic impedance (*Equation 9*), the propagation delay is approximately twice that of coaxial cable. Twisted pairs are used for backplane wiring, sometimes for driving differential receivers, and for breadboarding.

Wire Over Ground

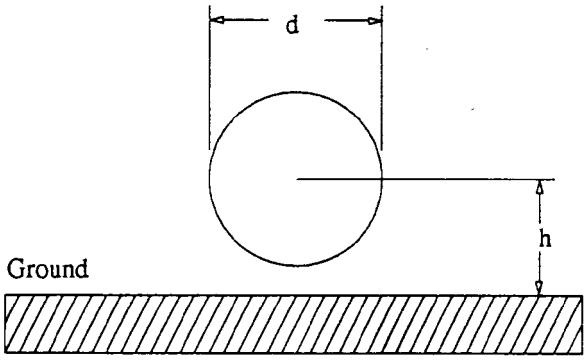
Figure 11 shows a wire over ground. This configuration is used for breadboarding and backplane wiring. The characteristic impedance is approximately 120Ω. This value can vary as much as ±40 percent, depending upon the distance from the groundplane, the proximity of other wires, and the configuration of the ground.

Microstrip Lines

A microstrip line (*Figure 12*) is a strip conductor (signal line) on a PCB separated from a ground plane by a dielectric. If the line's thickness, width, and distance from the ground plane are controlled, the line's characteristic impedance can be predicted with a tolerance of ±5 percent.

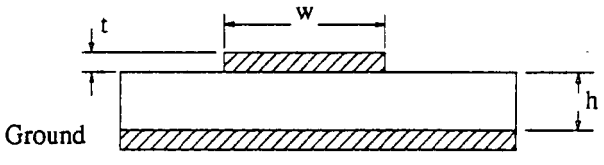
The formula given in *Figure 12* has proven to be very accurate for width-to-height ratios between 0.1:1 and 3.0:1 and for dielectric constants between 1 and 15.

The inductance per foot for microstrip lines is



$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4h}{d}\right)$$

Figure 11. Wire Over Ground



$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

Figure 12. Microstrip Line

$$L = (Z_O)^2 C_O \quad \text{Eq. 42}$$

where Z_O is the characteristic impedance and C_O is capacitance per foot.

The propagation delay of a microstrip line is

$$t_{pd} = 1.017\sqrt{0.45e_r + 0.67}(ns/ft) \quad \text{Eq. 43}$$

Note that the propagation delay depends only upon the dielectric constant and is not a function of the line width or spacing. For G-10 fiberglass epoxy PCBs (dielectric constant of 5), the propagation delay is 1.74 ns per foot.

Strip Lines

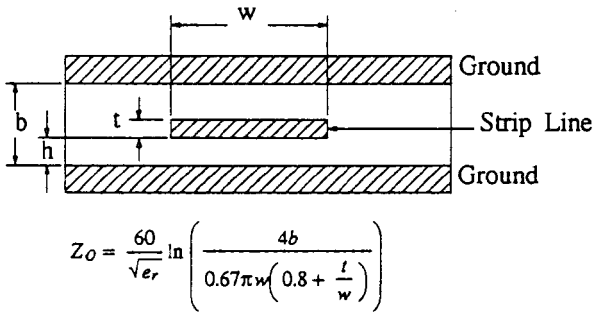
A strip line consists of a copper strip centered in a dielectric between two conducting planes (*Figure 13*). If the line's thickness, width, dielectric constant, and distance between ground planes are all controlled, the tolerance of the characteristic impedance is within ±5 percent. The equation given in is accurate for W/(b – t) < 0.35 and t/b < 0.25.

The inductance per foot is given by the formula

$$L = (Z_O)^2 C_O \quad \text{Eq. 44}$$

The propagation delay of the line is given by the formula

$$t_{pd} = 1.017\sqrt{e_r}(ns/ft) \quad \text{Eq. 45}$$



$$Z_O = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.67\pi w\left(0.8 + \frac{t}{w}\right)}\right)$$

Figure 13. Strip Line Construction

For G-10 fiberglass epoxy boards, the propagation delay is 2.27 ns per foot. The propagation delay is not a function of line width or spacing.

Modern PCBs

Most PCBs employ microstrip, stripline, or some combination of the two. Microstrip construction on a double-sided board with power and ground nets can suffice for low- to medium-performance, and low-density PCBs.

For high-performance, high-density PCBs, stripline construction is preferred. Power planes isolate signal layers from each other and provide higher-quality power and grounds than those of a two-layer board. Manufacturing quality control assures that the metalization is of uniform thickness and that the layers are properly laminated, thus ensuring uniform, predictable electrical characteristics.

When to Terminate Transmission Lines

Transmission lines should be terminated when they are long. From the preceding analysis, it should be apparent that

$$Long\ Line > \frac{t_r}{2t_{pdL}} \quad \text{Eq. 46}$$

where t_{pdL} is the loaded propagation delay of the line per unit length. For Cypress CMOS and BiCMOS products, the rise time, t_r, is typically 2 ns.

For stripline construction (multilayer PCBs), the line length at which voltage reflections might occur has been shown to vary from 4.73 inches for a 10-pF load to 3.05 inches for an 80-pF load (see *Equation 18* and *Table 1*).

Not all lines exceeding these lengths need to be terminated. Terminations are usually required on control lines (such as clock inputs, write and read strobe lines on SRAMs and FIFOs) and chip select or output-enable lines on RAMs, PROMs, and PLDs. Address lines and data lines on RAMs and PROMS usually have time to settle because they are normally not the highest-frequency lines in a system. However, if very heavily loaded, address and databus lines might require terminations.

Line Termination Strategies

There are two general strategies for transmission line termination:

1. Match the load impedance to the line impedance
2. Match the source impedance to the line impedance

In other words, if either the load reflection coefficient or the source reflection coefficient can be made to equal zero, reflections are eliminated. From a systems design viewpoint, strategy 1 is preferred. Eliminating the reflection at the load (i.e., dissipating the excess energy) before the energy travels back to the source causes less noise, electromagnetic interference (EMI), and radio frequency interference (RFI).

Multiple Loads, Buses, and Nodes

In the case where multiple loads are connected to a transmission line, only one termination circuit is required. The termination should be located at the load that is electrically the greatest distance from the source. This is usually the load that is the greatest physical distance from the source. A point-to-point or daisy chain connection of loads is preferred.

Bidirectional buses should be terminated at each end with a circuit whose impedance equals the intrinsic, characteristic line impedance. The reason is that each transmitting device sees the characteristic impedance of the line when the device is transmitting.

Consider next a line that has three bidirectional nodes: one on each end and one in the middle. The middle node, when driving the line, sees an impedance equal to $Z_O/2$, because the node is looking into two lines in parallel with each other. The end nodes, however, see an impedance of Z_O. In this case, as in a backplane, each end of the line should be terminated in an impedance equal to $Z_O/2$. When heavily loaded, *Equation 12* must be used to calculate the loaded characteristic impedance, and this must be used instead of Z_O.

Types of Terminations

There are three basic types of terminations: series damping, pull-up/pull-down, and parallel AC terminations. Each has its advantages and disadvantages.

Except for series damping, the termination network should be attached to the input (load) that is electrically the greatest distance from the source. Component leads should be as short as possible to prevent reflections due to lead inductance.

Series Damping

Series damping is accomplished by inserting a small resistor (typically 10Ω to 75Ω) in series with the transmission line, as close to the source as possible (*Figure 14*). Series damping is a special case of damping in which the series resistor value plus the circuit output impedance equals the transmission line impedance. The strategy is to prevent the wave reflected back from the load from reflecting back from the source. This is done by making the source reflection coefficient equal to zero.

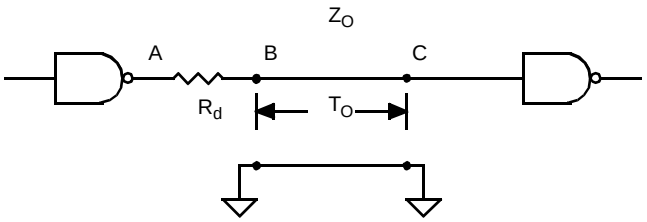


Figure 14. Series Damping Termination

The channel resistance (on resistance) of the pull-down device for Cypress ICs is 10Ω to 20Ω, depending upon the current-sinking requirements. Thus, subtract this value from the series-damping resistor, R_d.

$$Z_O = R_S + R_d \qquad \text{Eq. 47}$$

A disadvantage of the series-damping technique, as illustrated in *Figure 15*, is that during the two-way propagation delay time of the signal edges, the voltage at the input to the line is halfway between the logic levels, due to the voltage divider action of R_S. The "half voltage" propagates down the line to the load and then back from the load to the source. This means that no inputs can be attached along the line, because they would respond incorrectly during this time. However, you can attach any number of devices to the load end of the line because all the reflections are absorbed at the source. If two or more transmission lines must be driven in parallel, the value of the series-damping resistor does not change.

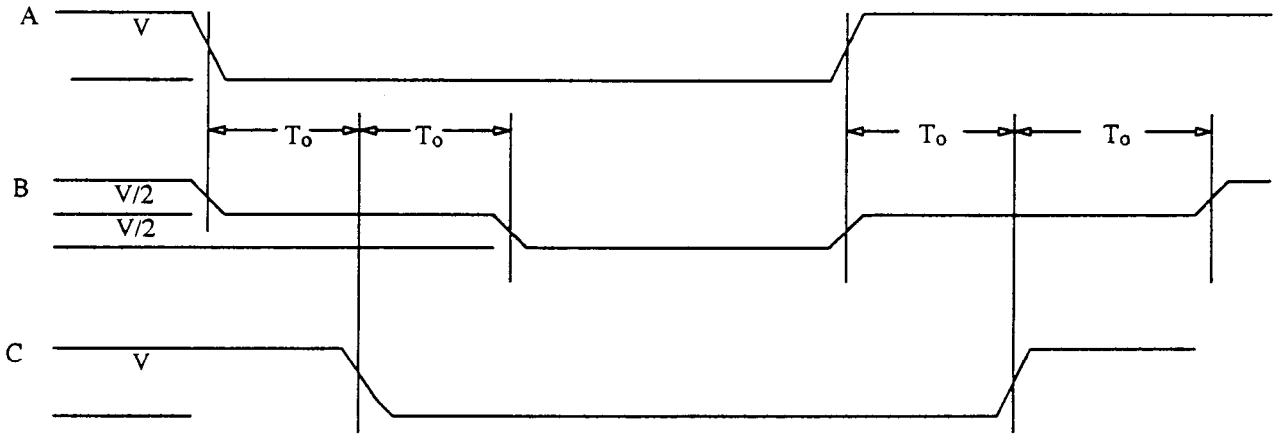


Figure 15. Series Damping Timing

The advantages of series termination are:

- Requires only one resistor per line
- Consumes little power
- Permits incident wave switching at the load after a T_O propagation delay

- Provides current limiting when driving highly capacitive loads; the current limiting also helps reduce groundbounce

The disadvantages of series termination are:

- Degrades rise time at the load due to increased RC time constant
- Should not be used with distributed loads

The low input current required by Cypress CMOS ICs results in essentially no DC power dissipation. The only AC power required is to charge and discharge the parasitic capacitances.

Pull-Up/Pull-Down Termination

The pull-up/pull-down resistor termination shown in *Figure 16* is included for historical reasons and for the sake of completeness. For TTL driving long cables, such as ribbon cables, the values R_1 = 220Ω and R_2 = 330Ω are recommended by several bus interface standards. If the cable is disconnected, the voltage at point B is 3V, which is well above the 2V minimum high TTL specification. Because most control signals are active LOW, a disconnected cable results in the unasserted state.

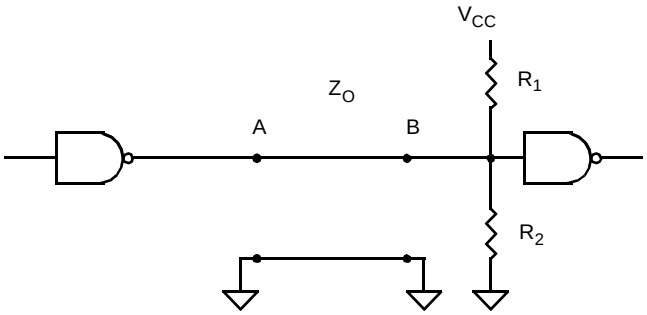


Figure 16. Pull-Up/Pull-Down

The maximum value of R_1 is determined by the maximum acceptable signal rise time, which is a function of the charging RC time constant. The minimum value of R_1 is determined by the amount of current the driver can sink. The value of R_2 is chosen such that a logic HIGH is maintained when the cable is disconnected. The equivalent Thévenin resistance is

$$R_T = \frac{R_1 R_2}{R_1 + R_2} \qquad \text{Eq. 48}$$

The value of R_1 and R_2 in parallel is slightly less than the cable's characteristic impedance. Ribbon cables with characteristic impedances of 150Ω are typical.

If both resistors are used, DC power is dissipated all the time. If only a pull-down resistor (R_2) is used, DC power is dissipated when the input is in the logic HIGH state. Conversely, if only a pull-up resistor (R_1) is used, power is dissipated when the input is in the LOW state. Due to these power dissipations, this termination is not recommended.

If an unterminated control signal on a PCB is suspected of causing a problem, a resistor whose value is slightly less than the characteristic impedance of the line (e.g., 47Ω) can be connected between the input pin and ground. Be sure that the driver can source sufficient current to develop a TTL high voltage level (2.0V) across the resistor.

In special cases where inputs should be either pulled up (HIGH) for logic reasons or because of very slow rise and fall times, you can use a pull-up resistor to V_{CC} in conjunction with the terminating network shown in *Figure 17*. DC power is dissipated when the source is LOW.

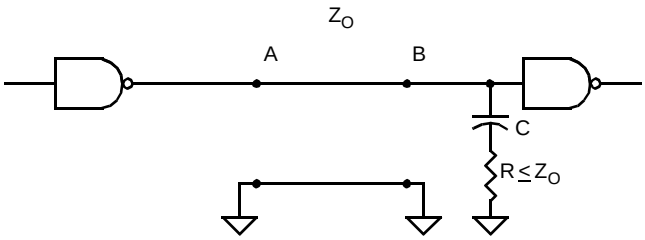


Figure 17. Parallel AC Termination

Parallel AC Termination

Figure 17 illustrates the recommended general-purpose termination. It does not have the disadvantage of the half-voltage levels of series damping terminations, and it causes no DC power dissipation. You can attach loads anywhere along the line, and they see a full voltage swing.

The disadvantage is that a parallel AC termination requires two components, versus the one-component series-damping termination.

Commercially Available RC Networks

A variety of combinations of R and C values are available as series RC networks in SIP packages from at least two sources.

Bourns calls these networks the Series 701 and 702 RC Termination Networks. You can obtain datasheets by calling the factory in Logan, Utah (801-750-7200) or a local sales office.

Thin Film Technology also refers to the networks as RC Termination Networks. You can obtain datasheets by calling the factory in North Mankato, Minnesota at 507-635-8445.

Dale Electronics calls their product Resistor/Capacitor Networks. Call 915-595-8139 for information.

California Micro Devices calls their product R–C Networks. Call 408-263-3214 for information.

Low-Pass Filter Analysis

The parallel AC termination has another advantage: it acts as a low-pass filter for short pulses. You can verify this by analyzing the response of the circuit illustrated in *Figure 18* to a positive and a negative step function. The positive step function is generated by moving the switch from position 2 to position 1. The negative step function is generated by moving the switch from position 1 to position 2. The response of the circuit to a pulse is the superposition of the two separate responses. The input impedance of the Cypress circuits connected to the termination network are so large that they can be ignored for this analysis.

Classic circuit analysis usually assumes an ideal source (R_1 = R_2 = 0). In real-world digital circuits, the source output impedance is not only non-zero, but also varies depending upon whether the output is changing from LOW to HIGH or vice versa.

For Cypress ICs, 100Ω > R_1 > 50Ω and 20Ω > R_2 > 10Ω, depending upon speed and output current-sinking requirements.

Positive Step Function Response

The initial voltage on the capacitor is zero. At t = 0, the switch is moved from position 2 to position 1. At t = 0+, the capacitor appears as a short circuit, and the voltage V is applied through R_1 to charge the load (R_3C). The voltage across the capacitor V_C(t), is

$$V_C(t) = V\left(1 - e^{\left[\frac{-t}{(R_1 + R_3)C}\right]}\right) \quad \text{Eq. 49}$$

In theory, the voltage across the capacitor reaches V when t equals infinity. In practice, the voltage reaches 98 percent of V after 3.9 RC time constants. You can verify this by setting V_C(t)/V = 0.98 in *Equation 49* and solving for t.

Negative Step Function Response

The capacitor is charged to approximately V. At t = 0, the switch is moved from position 1 to position 2, and the capacitor is discharged. The voltage across the capacitor, V_C(t) is

$$V_C(t) = Ve^{\left[\frac{-t}{(R_2 + R_3)C}\right]} \quad \text{Eq. 50}$$

The voltage decays to 2 percent of its original value in 3.9 RC time constants. You can verify this by setting V_C(t)/V =0.02 in *Equation 50* and solving for t.

The Ideal Case

Consider the ideal case where R_1 = R_2 = 0. Let R_3 = R in *Equations 49* and *50*. If a positive pulse of width T is applied to the modified circuit of *Figure 18*, the pulse disappears if 4RC > T.

Because the discharging time constant is the same as the charging time constant for the ideal case, a negative-going pulse of width T also disappears if 4RC > T. That is, if the applied signal is normally HIGH and goes LOW, as does the write strobe on an SRAM, the termination filters out all negative glitches less than 4 RC time constants in width.

The maximum frequency that the circuit passes is

$$F(max) = \frac{1}{2T} \quad \text{Eq. 51}$$

This is true because the charging and discharging time constants are equal for the ideal case.

Capacitance for the Ideal Case

The value of the capacitor, C, must be chosen to satisfy two conflicting requirements. First, the capacitor should be large enough to either absorb or supply the energy contained or removed when positive-going or negative-going glitches occur. Second, the capacitor should be small enough to avoid either delaying the signal beyond some design limit or slowing the signal rise and fall times to more than 5 ns.

A third consideration is the impedance caused by the capacitor's capacitive reactance, X_C. The digital waveforms applied to the AC termination can be expressed as a Fourier Series so that they can be manipulated mathematically. However, because these signals are not periodic in the classical meaning of the word, it is not clear that the AC steady-state analysis model of X_C applies here.

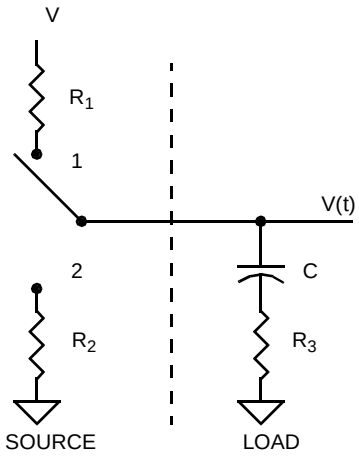


Figure 18. Lumped Load; AC Termination

In most applications, the degradation of the signal's rise and fall times beyond 5 ns determines the maximum value of the capacitor. The procedure is to calculate the rise time between the 10- and 90-percent amplitude levels, equate this rise time to 5 ns, and solve for C in terms of R:

$$V(t) = V\left(1 - e^{\left[\frac{-t}{RC}\right]}\right) \quad \text{Eq. 52}$$

for t yields

$$t = RC\ln\left[\frac{1}{1 - \frac{V(t)}{V}}\right] \quad \text{Eq. 53}$$

For $\frac{V(t)}{V} = 0.1, t = 0.10\ RC.$

For $\frac{V(t)}{V} = 0.9, t = 2.3\ RC.$

The time for the signal to transition from 10 to 90 percent of its final value is then T = 2.2 RC. Solving for C yields

$$C = \frac{T}{2.2R} \quad \text{Eq. 54}$$

For T = 5 ns, *Table 2* can be constructed. This table indicates that 50Ω transmission lines on PCBs that are terminated with RC networks should use a 47Ω resistor and a capacitor of 48 pF max; 47 pF is a standard value. This network eliminates glitches of 9 ns or less. The table's second column applies to wirewrapping construction, which is not recommended for systems operating at frequencies over 10 MHz. An exception is if the system consists of less than six MSI or SSI ICs.

Table 2. Termination Value for an Ideal Case

	PCB	Wirewrapped
Z_O (Ω)	50	120
R (Ω)	47	110

Table 2. Termination Value for an Ideal Case

C (max., pF)	48	20
RC (ns)	2.25	2.2
4RC (ns)	9	8.8

The Real World

To go from the ideal to the real world, calculate the values of R_1 and R_2 from the curves on the datasheet of the device driving the line. R_1 is the slope of the output source current vs. output voltage between 2 and 4V. R_2 is the slope of the output sink current vs. output voltage between 0 and 0.8V.

Add the value of R_1 to 47Ω and calculate C, using *Equation 54*. Then check to see that the RC charging time constant does not violate some minimum positive pulse-width specification for the line. If so, reduce C.

Add the value of R_2 to 47Ω and calculate C. Then check to see if the discharging RC time constant violates some minimum pulse-width specification for the line. If so, reduce C.

If the line is heavily loaded, *Equation 12* must be used to calculate the loaded characteristic impedance, which determines the maximum value of R. The Maximum value of C is then calculated using *Equation 54*.

Schottky Diode Termination

In some cases it can be expedient to use Schottky diodes or fast-switching silicon diodes to terminate lines. The diode switching time must be at least four times as fast as the signal rise time. Where line impedances are not well defined, as in breadboards and backplanes, the use of diode terminations is convenient and can save time.

A typical diode termination appears in *Figure 19*. The Schottky diode's low forward voltage, V_f (typically 0.3 to 0.45V), clamps the input signal to a V_f below ground (lower diode) and V_{CC} + V_f (upper diode). This significantly reduces signal undershoot and overshoot. Some applications may not require both diodes.

The advantages of diode terminations are:

- Impedance matched lines are not required
- The diodes replace terminating resistors or RC terminations

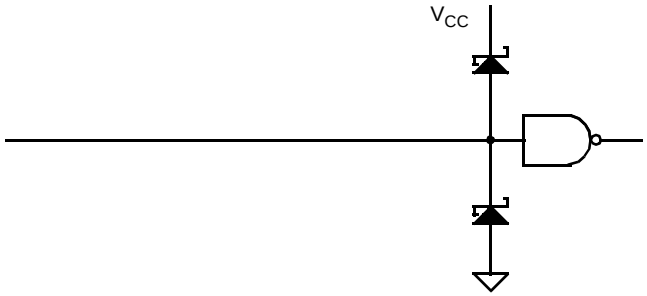


Figure 19. Schottky Diode Termination

- The diodes' clamping action reduces overshoot and undershoot
- Although diodes cost more than resistors, the total cost of layout might be less because a precise, controlled transmission-line environment is not required
- If ringing is discovered to be a problem during system debug, the diodes can be easily added

As with resistor or RC terminations, the leads should be as short as possible to avoid ringing due to lead inductance.

A few of the types of Schottky diodes commercially available are

- HSMS-2822 (Hewlett-Packard)
- 1N5711
- MBD101, MBD102 (Motorola)
- SN74S1050/52/56 (TI, single-diode arrays)
- SN74S1051/53 (TI, double-diode arrays)

Unterminated Line Example

The following example illustrates the procedure for calculating the waveforms when a Cypress PLD generates the write strobe for four Cypress FIFOs. The PLD is a PALC16L8 device and the FIFOs are CY7C429s.

The equivalent circuit appears in *Figure 20* and the unmodified driving waveform in *Figure 21*. The rise and fall times are 2 ns. The length of the stripline trace on the PCB is 8 inches and the intrinsic characteristic line impedance is 50Ω. The voltage waveforms at the source (point A) and the load (point B) must be calculated as functions of time. Stripline construction is used for this example because in most modern high-performance digital systems, the PCBs have multiple layers.

The equivalent ON channel resistance of the PLD pull-up device, 62Ω, is calculated using the output source current versus voltage graph, over the region of interest (2 to 4V), from the PALC20 series datasheet. The equivalent resistance of the pull-down device, 11Ω, is calculated in a similar manner, using the output sink current versus output voltage graph, over the region of interest (0.4 to 2V), also on the datasheet.

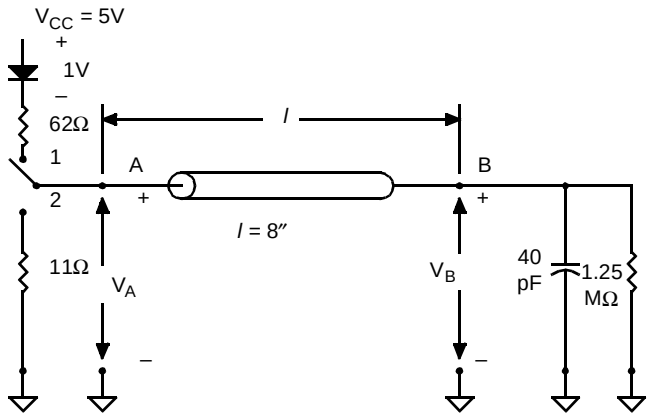


Figure 20. Equivalent Circuit for Cypress PAL Driving

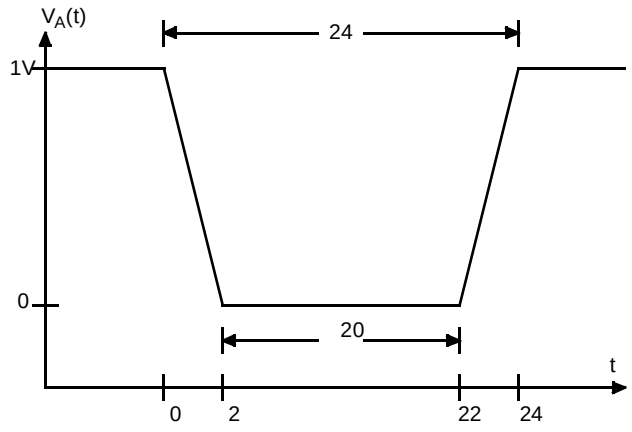


Figure 21. $V_A(t)$, Unmodified

The equivalent input circuit for the FIFO is constructed by approximating the input and stray capacitance with a 10-pF capacitor and the input resistance with a 5-MΩ resistor. The input leakage current for all Cypress products is specified as a maximum of ±10 μA, which guarantees a minimum of 500 KΩ at V_{in} = 5V. Typical leakage current is 10 pA.

Because the PLD is driving four FIFOs in parallel, the equivalent lumped capacitance is 4 x 10 pF = 40 pF, and the equivalent lumped resistance is 5,000,000/4 = 1.25 MΩ.

The next step is to calculate the propagation delay and the loaded characteristic impedance of the line. The unloaded propagation delay of the line is calculated using *Equation 45* with a dielectric constant of 5:

$$t_{pd} = 2.27(ns/ft) \quad \text{Eq. 55}$$

To calculate the loaded line propagation delay, the intrinsic capacitance must first be calculated using *Equation 9*.

$$t_{pd} = Z_O C_O \quad \text{Eq. 56}$$

where Z_O is the intrinsic characteristic impedance, and C_O is the intrinsic capacitance.

$$C_O = \frac{t_{pd}}{Z_O} = \frac{2.27\ ns/ft}{50} = 45.4\ pF/ft. \quad \text{Eq. 57}$$

Because the line is loaded with 40 pF, *Equation 11* is used to compute the loaded propagation delay of the line.

$$t_{pdL} = t_{pd}\sqrt{1 + C_D/C_O}$$

$$t_{pdL} = 2.27\ ns/ft \sqrt{1 + \frac{40\ pF}{45.4\ pF/ft \times \frac{8\ in}{12\ in/ft}}}$$

$$t_{pdL} = 3.46\ ns/ft \quad \text{Eq. 58}$$

Note that the capacitance per unit length must be multiplied by the line length to arrive at an equivalent lumped capacitance.

The intrinsic line impedance is reduced by the same factor by which the propagation delay is increased (1.524; see *Equation 12*):

$$Z_O' = \frac{50\Omega}{1.524} = 32.8\Omega \quad \text{Eq. 59}$$

Initial Conditions

At time t = 0, the circuit shown in *Figure 20* is in a quiescent state. The voltage at points A and B must be the same. By inspection:

$$V_A = V_B = (V_{CC} - Vf)\left(\frac{R_L}{R_S + R_L}\right)$$

$$= (5-1)\left(\frac{1.25 \times 10^6}{28 + 1.25 \times 10^6}\right) = 4V \quad \text{Eq. 60}$$

At t = 0, the driving waveform changes from 4V to approximately 0V with a fall time of 2 ns. This is shown in *Figure 20* by the switch arm moving from position 1 to position 2.

The wave propagates to the load at the rate of 3.46 ns per foot and arrives there

$$T_O = 3.46\ ns/ft \times \frac{8\ in.}{12\ in./ft} = 2.3\ ns \quad \text{Eq. 61}$$

later, as illustrated in *Figure 22b*.

Because the reflection coefficient at the load is ρL = 1, an early equal and opposite polarity waveform is propagated back to the source from the load. The reflection arrives at t =2T_O = 4.6 ns (*Figure 22a*). Note that the fall time is preserved.

The reflection coefficient at the source is

$$\rho_S = \frac{R_S - Z_O'}{R_S + Z_O'} = \frac{11 - 32.8}{11 + 32.8} = -0.498 \quad \text{Eq. 62}$$

To simplify the calculations that follow, consider –0.5 to be the low-level source reflection coefficient. The magnitude of the reflected voltage at the source is then

$$V_{S1} = -4V \times (-0.5) = 2V \quad \text{Eq. 63}$$

This wave propagates from the source to the load and arrives at t = 3 T_O. The wave adds to the 0V signal. The rise time is preserved, and thus the time required for the signal to go from 0 to 2V is

$$t_r = \frac{2V \times 2\ ns}{4V} = 1\ ns \quad \text{Eq. 64}$$

The signal at the load thus reaches the 2V level at time

$$t = 3T_O + 1\ ns = 7.9\ ns \quad \text{Eq. 65}$$

and remains at that level until the next reflection occurs at

$$t = 5T_O \quad \text{Eq. 66}$$

The wave that arrives at the load at 3 T_O reflects back to the source and arrives at

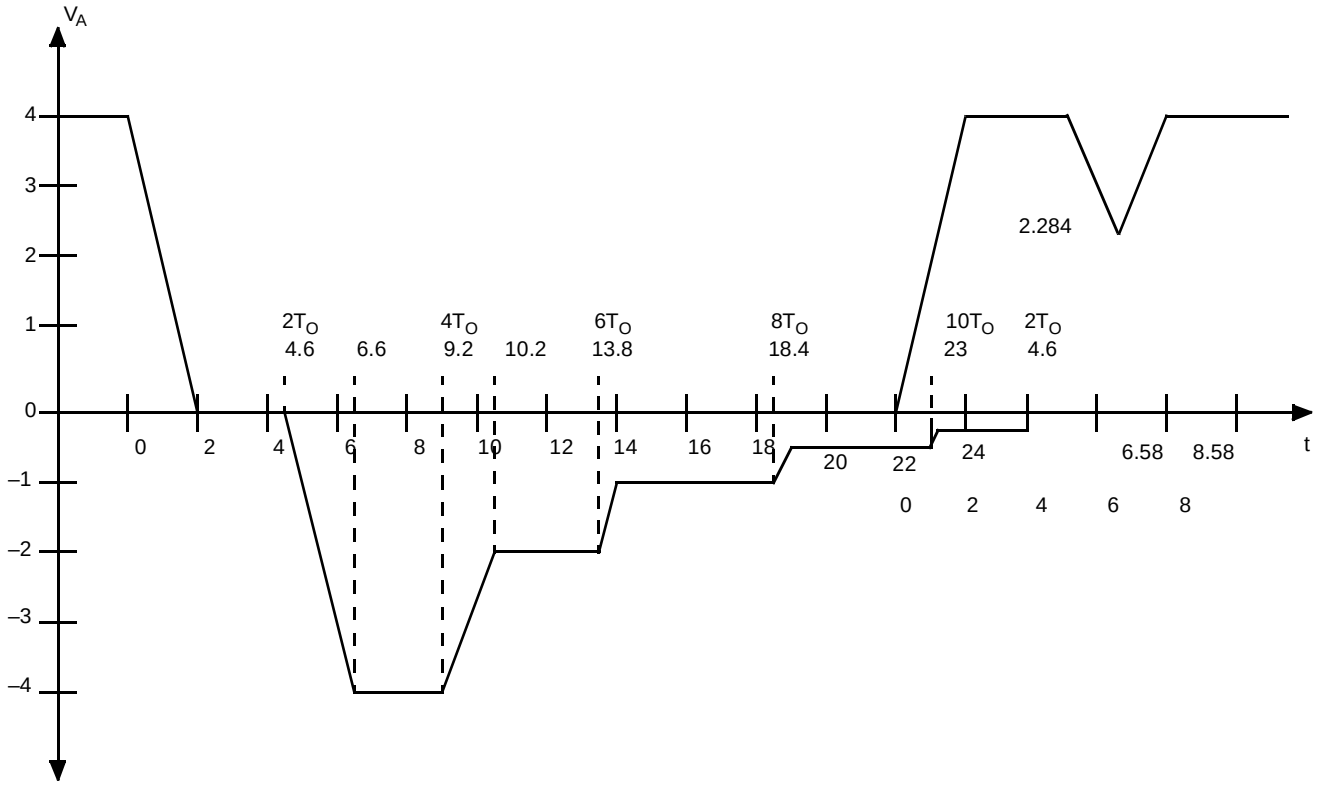


Figure 22a. Unterminated Line Example; $V_A(t)$

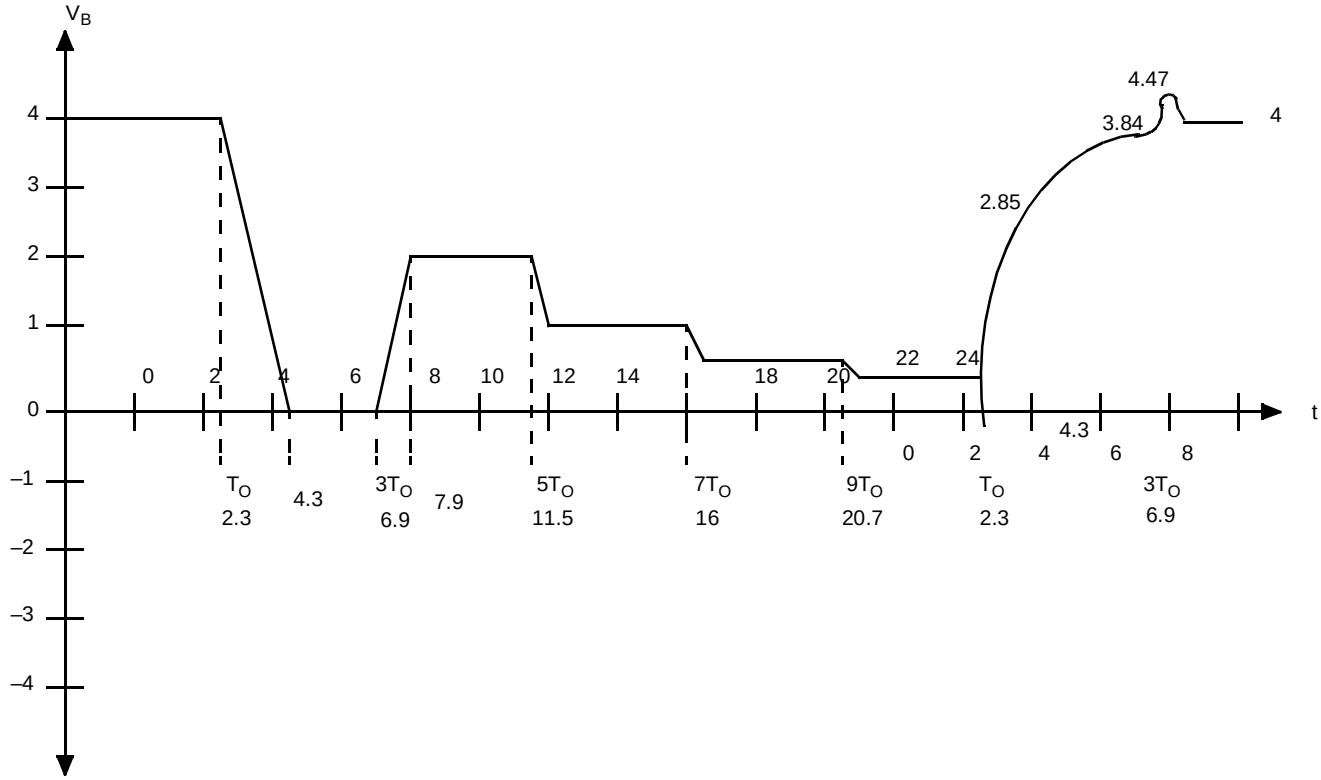


Figure 22b. Unterminated Line Example; $V_B(t)$

$$t = 4T_O = 9.2\ ns \quad \text{Eq. 67}$$

The 2V level adds to the –4V level, for a total of –2V. The rise time is preserved, so that this level is reached at

$$t = 4T_O + 1\ ns = 10.2\ ns \quad \text{Eq. 68}$$

and maintained until the next reflection occurs at

$$t = 6T_O \quad \text{Eq. 69}$$

The 2V wave that arrives at the source at $t = 4T_O$ reflects back to the load and arrives at $t = 5T_O$. The portion that is reflected back to the load is

$$V_{S2} = 2 \times (-0.5) = -1V \quad \text{Eq. 70}$$

This value subtracts from the 2V level to give 2 – 1 = 1V. Because the fall time is preserved, the time required for the signal to go from 2 to 1V is

$$t_f = \frac{1V \times 2\ ns}{4V} = 0.5\ ns \quad \text{Eq. 71}$$

The 1V level is thus reached at time

$$t = 5T_O + 0.5\ ns = 12\ ns \quad \text{Eq. 72}$$

At $t = 6T_O$, the 1V wave arrives back at the source, where it subtracts from the –2V level to give –1V. The rise time is

$$t_r = 1 \times 0.5\ ns/V = 0.5\ ns \quad \text{Eq. 73}$$

The signal at the source reaches the –1V level at

$$t = 6T_O + 0.5 = 14.3\ ns \quad \text{Eq. 74}$$

The 1V wave that arrives at the source at $t = 6T_O$ is reflected back to the load and arrives at $t = 7T_O$. The portion that is reflected back is

$$V_{S3} = 1 \times (-0.5) = -0.5V \quad \text{Eq. 75}$$

This value subtracts from the 1V level to give 0.5V. The fall time is 0.25 ns. The 0.5V level remains until the next reflection reaches the load at

$$t = 9T_O \quad \text{Eq. 76}$$

At $t = 8T_O$ the 0.5V wave that reflects from the load at $t= 7T_O$ arrives back at the source, where it subtracts from the –1V level to give –0.5V. The rise time is 0.25 ns. The portion that reflects back to the load is

$$V_{S4} = 0.5 \times (-0.5) = -0.25V \quad \text{Eq. 77}$$

The –0.25V signal arrives at the load at $t = 10T_O = 23$ ns and subtracts from the 0.5V signal to give 0.25V.

This process continues until the voltages at points A and B decay to approximately 0V.

Observations

The positive reflection coefficient at the load and the negative reflection coefficient at the source result in an oscillatory behavior that eventually decays to acceptable levels. The voltage at point A reaches –1V after $6T_O$ delays and the voltage at point B reaches 0.5V after $7T_O$ delays.

The reflection at the load that causes the voltage to equal the TTL minimum one level (2V) at $T = 3T_O$ causes a problem. The actual input voltage threshold level is 1.5V for TTL-compatible devices that do not exhibit hysteresis.

The voltage at the load falls from 4V to 0V in 2 ns, beginning at $t = T_O$. Because $T_O = 2.3$ ns, the voltage reaches zero at

$$2.3\ ns + 2\ ns = 4.3\ ns \quad \text{Eq. 78}$$

The 1.5V level occurs at

$$4.3\ ns - \frac{2\ ns}{4V} \times 1.5V = 3.55\ ns \quad \text{Eq. 79}$$

The rising edge begins at

$$t = 3T_O = 6.9\ ns \quad \text{Eq. 80}$$

The 1.5V level occurs at

$$6.9\ ns + \frac{2\ ns}{4V} \times 1.5 = 7.65\ ns \quad \text{Eq. 81}$$

The time difference (7.65 – 3.55 = 4.1 ns) is long enough for the FIFO to interpret the signal as a LOW.

Next, consider the width of the positive pulse that begins at the load at $t = 3T_O$. Because the rise time is preserved, the signal takes 1 ns to reach 2V, or 0.75 ns to reach 1.5V. The signal begins to fall at $t = 5T_O$, reaching 1.5V at

$$t = 5T_O + 0.25\ ns = 11.75\ ns \quad \text{Eq. 82}$$

The difference (11.75 – 7.65) is 4.1 ns, which is wide enough for the FIFO to interpret as a second clock. To eliminate this pulse, the line must be terminated.

Strobe Shortening Considerations

In this example the width of the negative strobe is 22 to 24 ns. If a CY7C429-20 FIFO is used, the write (or read) strobe must not be shorter than 20 ns. Even if the FIFO does not recognize the 4.5-ns negative pulse, the shortening of the write strobe by $5T_O = 11.5$ ns is sufficient to violate the minimum negative-pulse-width specification.

This strobe-shortening phenomenon might also occur on other active-LOW control lines such as output enables and chip selects. Clock lines must also be analyzed for this problem; in general, these lines should be terminated.

Now consider an analysis of the write strobe's rising edge to assure that the reflections associated with this edge do not cause multiple clocks or false triggering of the FIFO. At t = 22 ns, the rising edge of the write strobe begins, which is the equivalent of closing the switch in *Figure 20* in the 1 position. For this analysis, it is convenient to start the timescale over at zero, as appears in *Figure 22a* and *Figure 22b*.

If the forcing function were a step function, the equations of *Figure 4h* would apply. The time constant in the equation is

$$T = \frac{RZ_O'C_e}{R + Z_O'} \quad \text{Eq. 83}$$

Because

$$R > Z_O', T = Z_O'C_e \quad \text{Eq. 84}$$

where Z_O' = 32.8Ω, and C_e = 45.4 pF.

This is the equivalent of saying that you can ignore the1.25-MΩ device input resistance for transient circuit analysis. Substituting Z_O' and C_e into the preceding equation yields a time constant of T = 1.489 ns.

Writing the equation for the voltages for the circuit of *Figure 20* yields

$$V_B(t) = iZ_O' + \frac{1}{C_e}\int_0^t idt \quad \text{Eq. 85}$$

Also,

$$V_B(t) = K_tU(t) - K(t-T1)U(t-T1) \quad \text{Eq. 86}$$

where K_t is the rising edge of the write strobe (K = 2V/ns) applied at t = 0 using a unit step function, U(t); and –K(t – T1) represents an equal but opposite waveform applied at t = T1 (after the rise time) using a unit step function, U(t – T1).

Equating the expressions and taking the LaPlace transforms of both sides yields

$$\frac{K}{s^2} - \frac{Ke^{-T1s}}{s^2} = Z_O'I(s) + \frac{I(s)}{C_es} = \left(Z_O' + \frac{1}{C_es}\right)I(s) \quad \text{Eq. 87}$$

However,

$$V_B(t) = \frac{1}{C_e}\int_0^t idt \qquad or, V_B(s) = \frac{I(s)}{C_es} \quad \text{Eq. 88}$$

Therefore,

$$\frac{K}{s^2} - \frac{Ke^{-T1s}}{s^2} = \left(Z_O' + \frac{1}{C_es}\right)C_esV_B(s) \quad \text{Eq. 89}$$

Solving for V_B(s) yields

$$V_B(s) = \frac{\frac{K}{s^2}(1-e^{-T1s})}{C_es\left(Z_O' + \frac{1}{C_es}\right)} \quad \text{Eq. 90}$$

which is equivalent to

$$\frac{\frac{K}{Z_O'C_e}(1-e^{-T1s})}{s^2\left(s + \frac{1}{Z_O'C_e}\right)} \quad \text{Eq. 91}$$

Taking the inverse LaPlace transform yields

$$V_B(t) = \left[KZ_O'C_e\left(e^{\frac{-t}{Z_O'C_e}} - 1\right) + K_t\right]U(t) - \left[KZ_O'C_e\left(e^{\left(\frac{-(t-T1)}{Z_O'C_e}\right)} - 1\right) + K(t-T1)\right]U(t-T1) \quad \text{Eq. 92}$$

The first term in *Equation 92* applies from time zero up to and including T1, and the second term applies after T1:

$$V_B(t) = \frac{KZ_O'C_e}{T1}\left(e^{\left[\frac{-t}{Z_O'C_e}\right]} - 1\right) + \frac{K}{T1}(t) \quad \text{Eq. 93}$$

for t ≤ T1.

$$V_B(t) = \frac{KZ_O'C_e}{T1}\left(1 - e^{\left[\frac{T1}{Z_O'C_e}\right]}\right)e^{\left[\frac{-t}{Z_O'C_e}\right]} + K1 \quad \text{Eq. 94}$$

for t > T1.

where K1 is the final value, which is 4V.

Substituting the correct values for t = T1 = 2 ns yields

$$V_B(t = T1) \quad \text{Eq. 95}$$

$$= \frac{2 \times 32.8 \times 45.4 \times 10^{-12}}{2 \times 10^{-9}}(\varepsilon^{-1.489} - 1) + \frac{2V}{ns} \times 2\ ns$$

$$= -1.15 + 4 = 2.85V$$

If the forcing function is a step function, the equation is

$$V_B(t) = 4V\left(1 - e^{\left[\frac{-t}{Z_O'C_e}\right]}\right) \quad \text{Eq. 96}$$

at t = 2 ns, V_B = 3V, which is more than the 2.85V calculated using *Equation 93*.

At t = 22 ns + T_O, the voltage waveform begins to build up at the load and continues to build until the first reflection from the source occurs at t = 3T_O.

Equation 94 is used to calculate the voltage at the load at t = 2T_O, because 1T_O is used for propagation delay time:

$$V_B(t = 2T_O) \quad \text{Eq. 97}$$

$$= \frac{-2V \times 32.8 \times 45.4 \times 10^{-12}}{2 \times 10^{-9}}(1 - e^{-1.489})(e^{-2}) + 4$$

$$= -1.489(0.774)(0.1353) + 4$$

$$= -1.559 + 4 = 3.84V$$

The voltage at the load remains at this value until the first reflection from the source reaches the load at t = 3T_O.

Meanwhile, at t = T_O, the wave at the load reflects back to the source and arrives at t = 2T_O. The wave subtracts from the 4V

level at the source, as illustrated in *Figure 6c*. The amplitude of the droop is given by

$$V_r = \frac{C' Z_O' V_O}{2 T_r} \quad \text{Eq. 98}$$

for $R_S = Z_O$.

If R_S does not equal Z_O', *Equation 98* must be modified. Instead of $V_O/2$, the voltage is

$$V_O\left(\frac{R_S}{R_S + Z_O'}\right) \quad \text{Eq. 99}$$

so that *Equation 98* becomes

$$V_r = \frac{C' Z_O' V_O}{T_r}\left(\frac{R_S}{R_S + Z_O'}\right) \quad \text{Eq. 100}$$

where $C' = 40$ pF, $Z_O' = 32.8\Omega$, $R_S = 62\Omega$, $T_r = 2$ ns, and $V_O = 4$V. Substituting these values into *Equation 100* yields

$$V_r = 1.716V \quad \text{Eq. 101}$$

Because 4V – 1.716 = 2.284, the voltage does not drop below the minimum TTL V_{IH} level of 2V, but it does come close.

The reflection coefficient at the source is

$$\rho_S = \frac{R_S - Z_O'}{R_S + Z_O'} \quad \text{Eq. 102}$$

where, $R_S = 62$ ohms, $Z_O' = 32.8$ ohms, $\rho_s = 0.308$.

The amount of voltage reflected from the source back to the load is then

$$V_{S1} = 1.716 \times 0.308 = 0.53V \quad \text{Eq. 103}$$

The 40-pF capacitor reduces the rise time of the waveform at the load. The reflection at the source caused by the load capacitor is insufficient to reduce the 4V level to less than the TTL one level (2V).

The reflection coefficient at the source is small enough so that the energy reflected back to the load is insufficient to cause a problem.

References

1. Matick, Richard E. *Transmission Lines for Digital and Communications Networks*. McGraw Hill, 1969.
2. Blood, Jr., William R. *MECL System Design Handbook*. Motorola Inc., 1983.