DIGITAL SYSTEMS
MODEL FDC-1
FLOPPY DISK CONTROLLER
INTERFACE MANUAL

DIGITAL SYSTEMS
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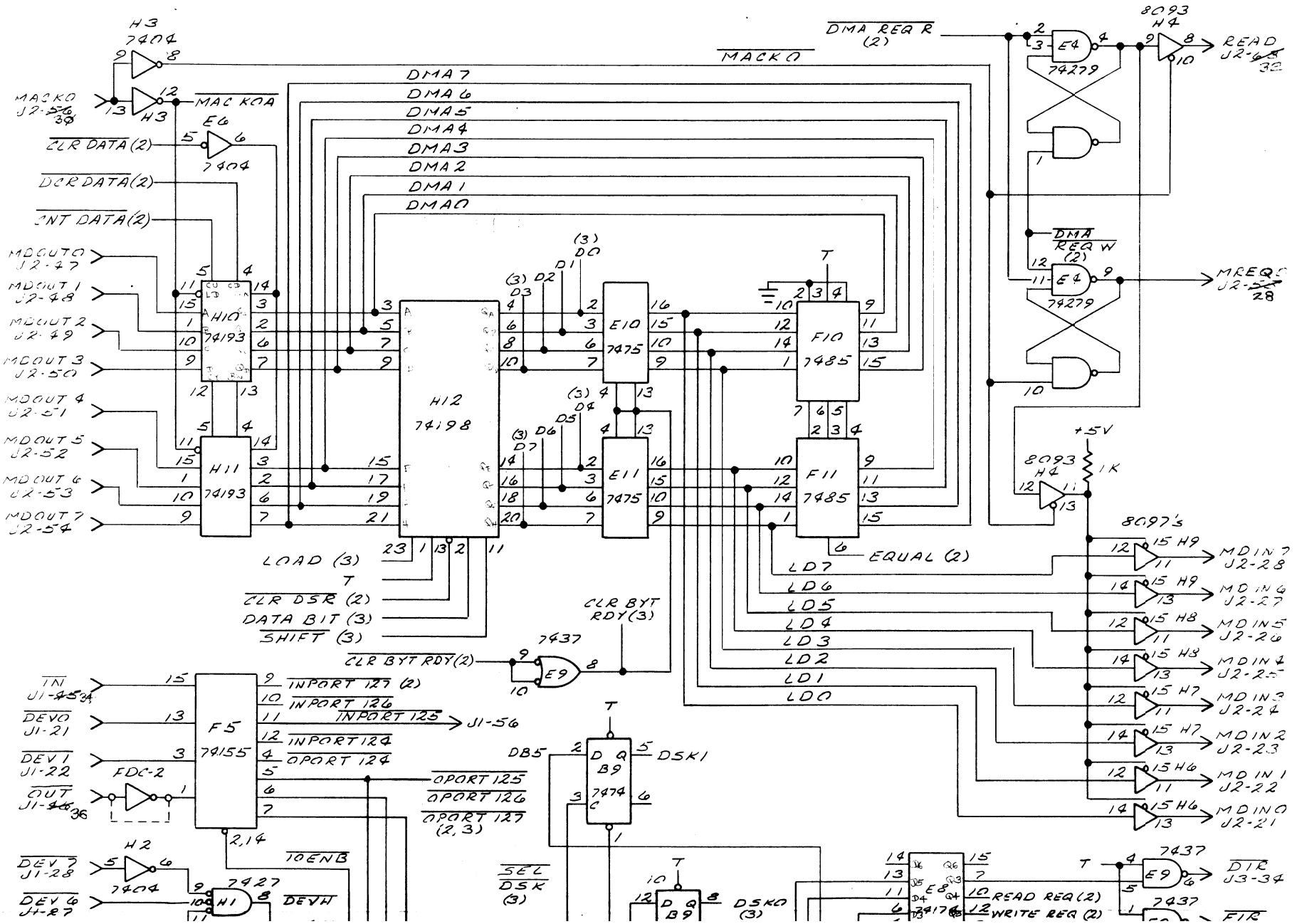
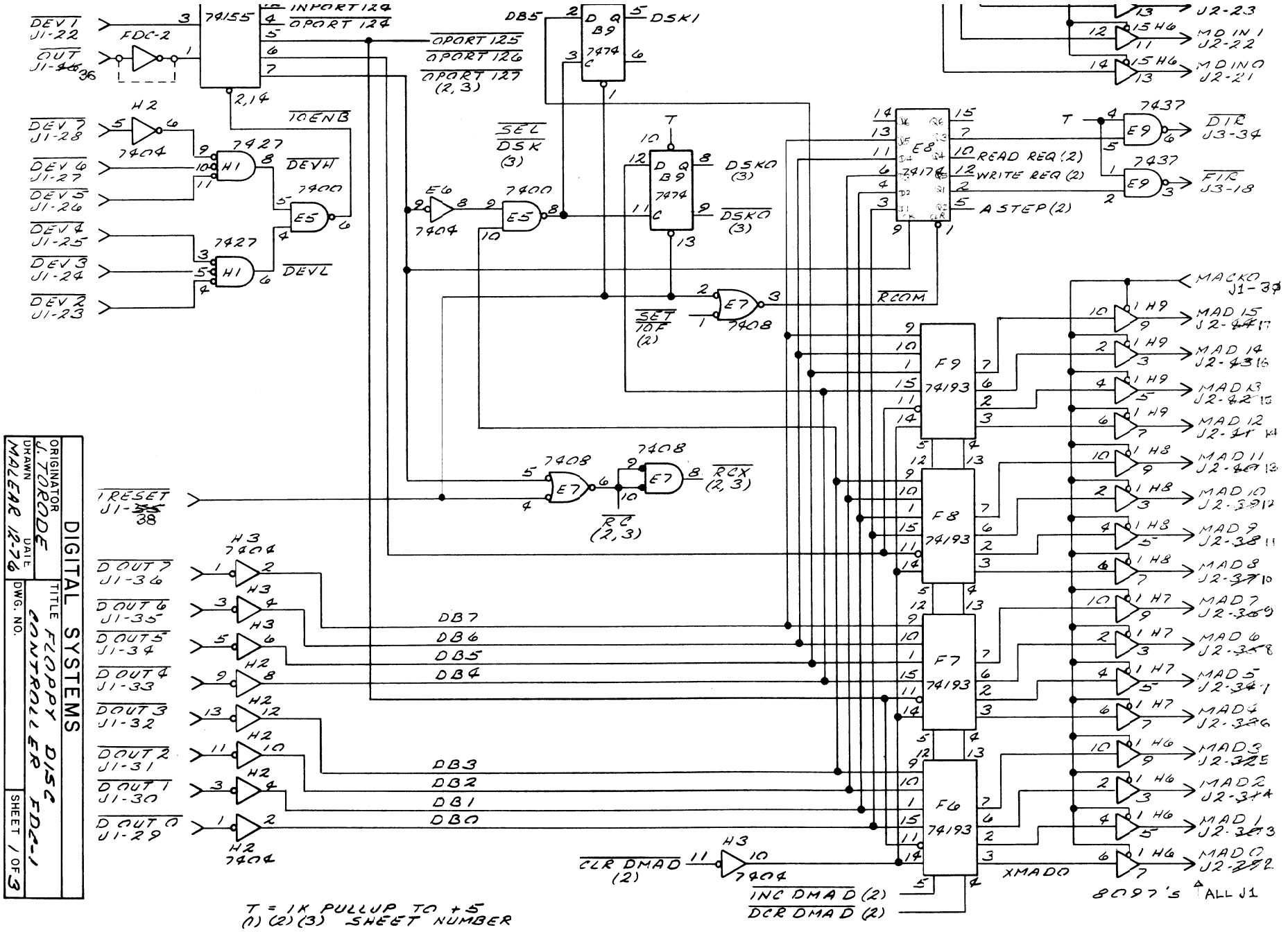
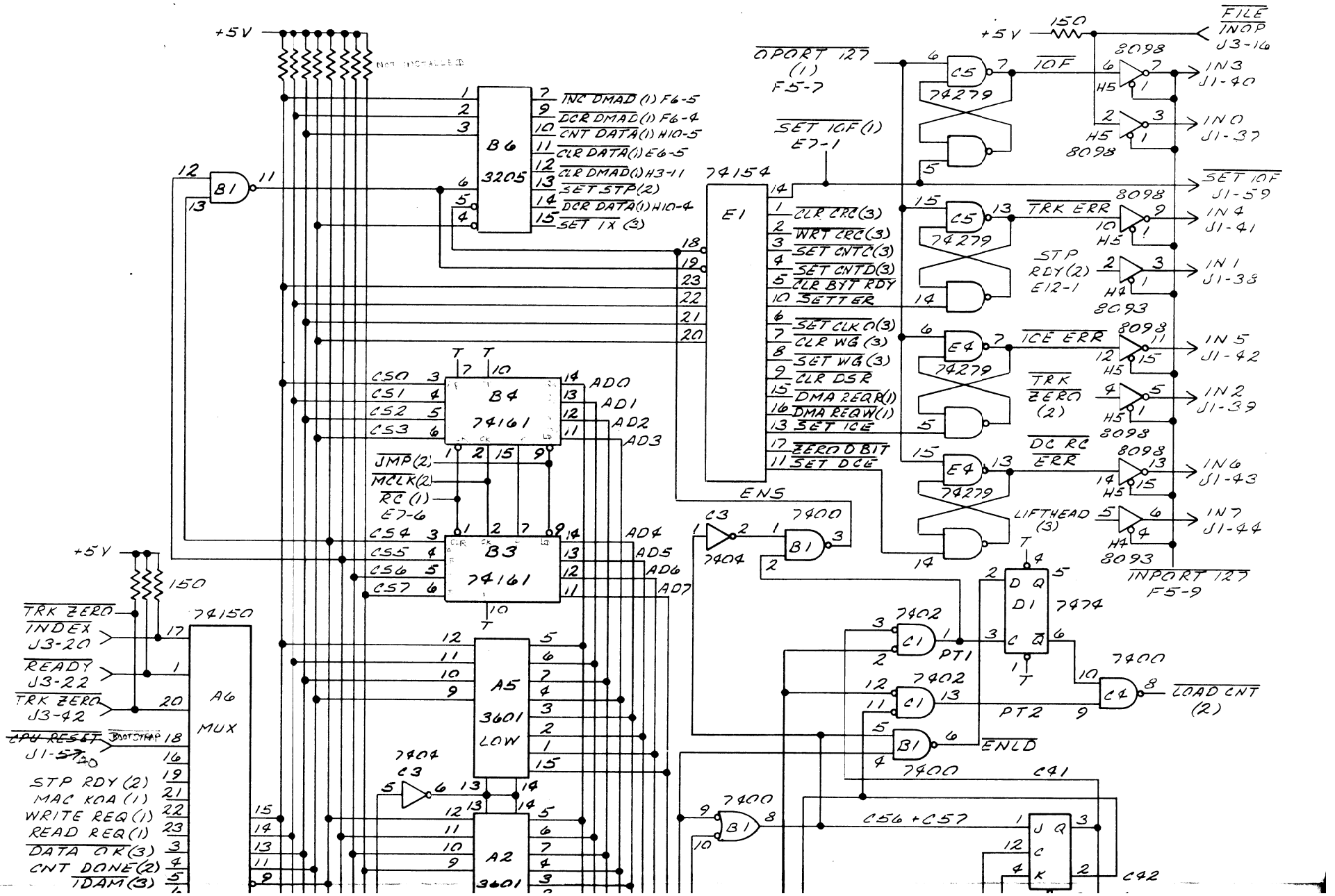
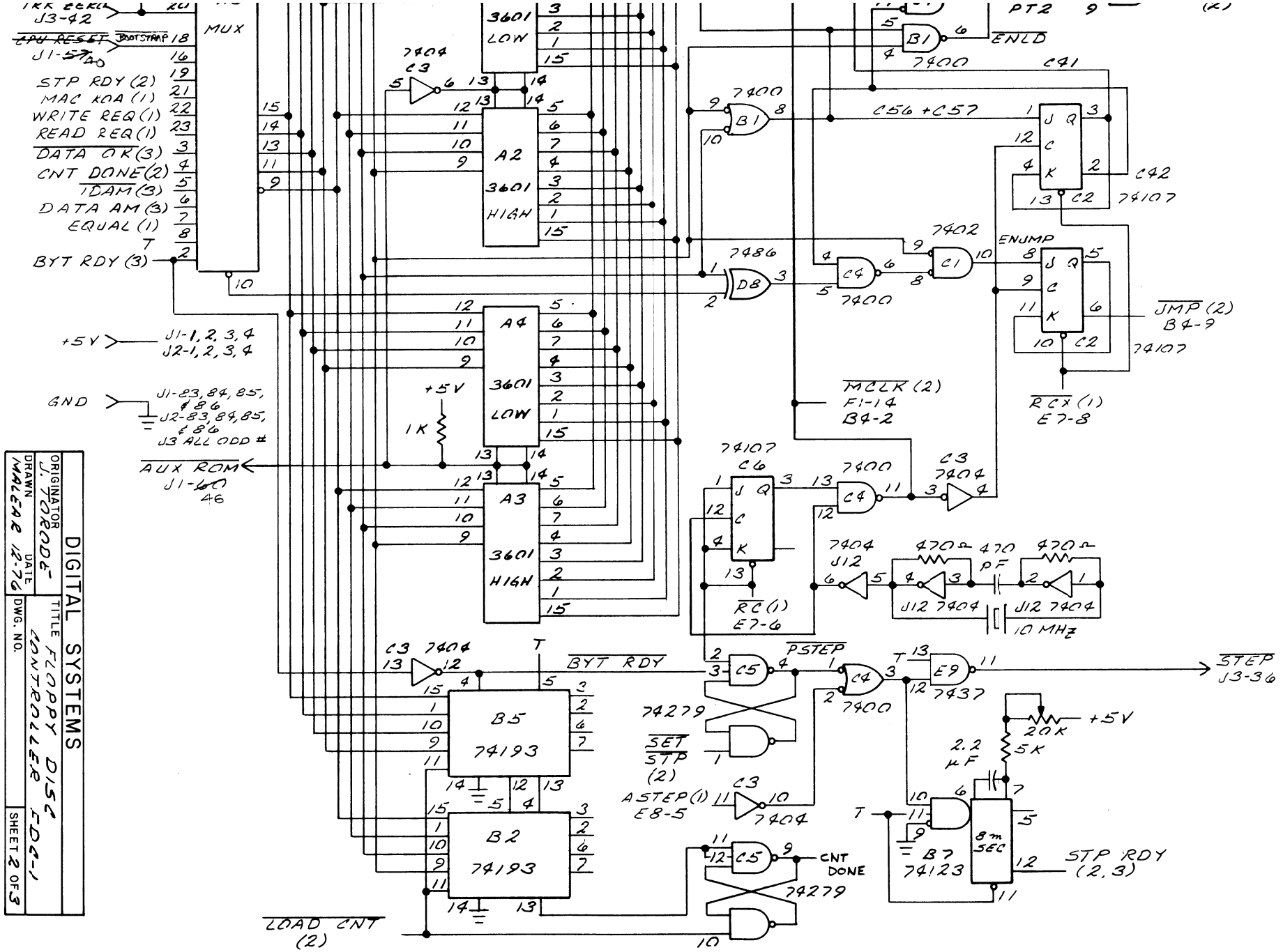

H3 7404
MACKO J2-56 39
MAC KOA
E6 7404
CLR DATA (2)
DCR DATA (2)
CNT DATA (2)
MDOUT0 J2-47
MDOUT1 J2-48
MDOUT2 J2-49
MDOUT3 J2-50
MDOUT4 J2-51
MDOUT5 J2-52
MDOUT6 J2-53
MDOUT7 J2-54
H10 74193
H11 74193
H12 74198
DMA7
DMA6
DMA5
DMA4
DMA3
DMA2
DMA1
DMA0
MACKO
DMA REQ R (2)
E4 74279
8093 H4
READ J2-38
DMA REQ W (2)
MREQ J2-28
+5V
1K
E10 7475
F10 7485
E11 7475
F11 7485
LOAD (3)
T
CLR DSR (2)
DATA BIT (3)
SHIFT (3)
CLR BYT RDY (3)
CLR BYT RDY (2)
7437 E9
EQUAL (2)
LD7
LD6
LD5
LD4
LD3
LD2
LD1
LD0
8097's
MDIN7 J2-28
MDIN6 J2-27
MDIN5 J2-26
MDIN4 J2-25
MDIN3 J2-24
MDIN2 J2-23
MDIN1 J2-22
MDIN0 J2-21
IN J1-45 34
DEVO J1-21
DEV1 J1-22
OUT J1-46 36
FDC-2
F5 74155
INPORT 127 (2)
INPORT 126
INPORT 125 J1-56
INPORT 124
OPORT 124
OPORT 125
OPORT 126
OPORT 127 (2,3)
DB5
DSK1
B9 7474
SEL DSK (3)
DSK0 (3)
DEV7 J1-28
DEV6 J1-27
H2 7404
H1 7427
DEVH
IOENB
READ REQ (2)
WRITE REQ (2)
DIR J3-34
FIR


DEV1 J1-22
OUT J1-36
FDC-2
74155
INPORT 124
OPORT 124
OPORT 125
OPORT 126
OPORT 127 (2,3)
2,14
IOENB
DEV7 J1-28
DEV6 J1-27
DEV5 J1-26
DEV4 J1-25
DEV3 J1-24
DEV2 J1-23
7404
7427
DEVH
DEVL
7400
DB5
DSK1
SEL DSK (3)
DSKO (3)
SET 10F (2)
7408
RCOM
READ REQ (2)
WRITE REQ (2)
ASTEP (2)
7437
DIR J3-34
FIR J3-18
MACKO J1-34
MAD15 J2-17
MAD14 J2-16
MAD13 J2-15
MAD12 J2-14
MAD11 J2-13
MAD10 J2-12
MAD9 J2-11
MAD8 J2-10
MAD7 J2-9
MAD6 J2-8
MAD5 J2-7
MAD4 J2-6
MAD3 J2-5
MAD2 J2-4
MAD1 J2-3
MAD0 J2-2
MDIN1 J2-22
MDIN0 J2-21
J2-23
IRESET J1-38
RCX (2,3)
RC (2,3)
DOUT7 J1-36
DOUT6 J1-35
DOUT5 J1-34
DOUT4 J1-33
DOUT3 J1-32
DOUT2 J1-31
DOUT1 J1-30
DOUT0 J1-29
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
CLR DMAD (2)
INC DMAD (2)
DCR DMAD (2)
XMADO
8097's
ALL J1
T = 1K PULLUP TO +5
(1) (2) (3) SHEET NUMBER
ORIGINATOR J. TORODE
DRAWN MALEAR 12-76
DATE
DIGITAL SYSTEMS
TITLE FLOPPY DISC CONTROLLER FDC-1
DWG. NO.
SHEET 1 OF 3


+5V
NOT INSTALLED
B6
3205
INC DMAD (1) F6-5
DCR DMAD (1) F6-4
CNT DATA (1) H10-5
CLR DATA (1) E6-5
CLR DMAD (1) H3-11
SET STP (2)
DCR DATA (1) H10-4
SET IX (3)
B1
E1
74154
CLR CRC (3)
WRT CRC (3)
SET CNTC (3)
SET CNTD (3)
CLR BYT RDY
SETTER
SET CLK 0 (3)
CLR WG (3)
SET WG (3)
CLR DSR
DMA REQR (1)
DMA REQW (1)
SET ICE
ZERO D BIT
SET DCE
ENS
B4
74161
B3
74161
CS0
CS1
CS2
CS3
CS4
CS5
CS6
CS7
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
JMP (2)
MCLK (2)
RC (1)
E7-6
A5
3601
LOW
A2
3601
A6
MUX
74150
150
TRK ZERO
INDEX
J3-20
READY
J3-22
TRK ZERO
J3-42
CPU RESET
BOOTSTRAP
J1-50
STP RDY (2)
MAC KOA (1)
WRITE REQ (1)
READ REQ (1)
DATA OR (3)
CNT DONE (2)
IDAM (3)
7404
7400
7402
7474
OPORT 127
(1)
F5-7
SET IOF (1)
E7-1
IOF
TRK ERR
ICE ERR
DC RC
ERR
TRK
ZERO
(2)
STP
RDY (2)
E12-1
LIFTHEAD
(3)
8098
8093
74279
IN3
J1-40
IN0
J1-37
SET IOF
J1-59
IN4
J1-41
IN1
J1-38
IN5
J1-42
IN2
J1-39
IN6
J1-43
IN7
J1-44
FILE
INOP
J3-16
INPORT 127
F5-9
PT1
PT2
ENLD
LOAD CNT
(2)
C41
C56 + C57
C42


MUX
BOOTSTRAP
STP RDY (2)
MAC XOA (1)
WRITE REQ (1)
READ REQ (1)
DATA OK (3)
CNT DONE (2)
IDAM (3)
DATA AM (3)
EQUAL (1)
BYT RDY (3)
+5V
GND
AUX ROM
3601 LOW
3601 HIGH
A1
A2
A3
A4
B1
B2
B5
C1
C2
C3
C4
C5
C6
D8
74193
74279
74107
7400
7402
7404
7437
7486
1K
470Ω
470 pF
10 MHz
20K
5K
2.2 μF
8m SEC
B7 74123
PT2
ENLD
C41
C56 + C57
C42
ENJMP
JMP (2) B4-9
MCLK (2) F1-14 B4-2
RCX (1) E7-8
RC (1) E7-6
PSTEP
STEP J3-36
BYT RDY
SET STP (2)
ASTEP (1) E8-5
CNT DONE
STP RDY (2, 3)
LOAD CNT (2)
J3-42
J1-50
J1-1, 2, 3, 4
J2-1, 2, 3, 4
J1-83, 84, 85, & 86
J2-83, 84, 85, & 86
J3 ALL ODD #
J1-60
46
DIGITAL SYSTEMS
ORIGINATOR J. CORODE
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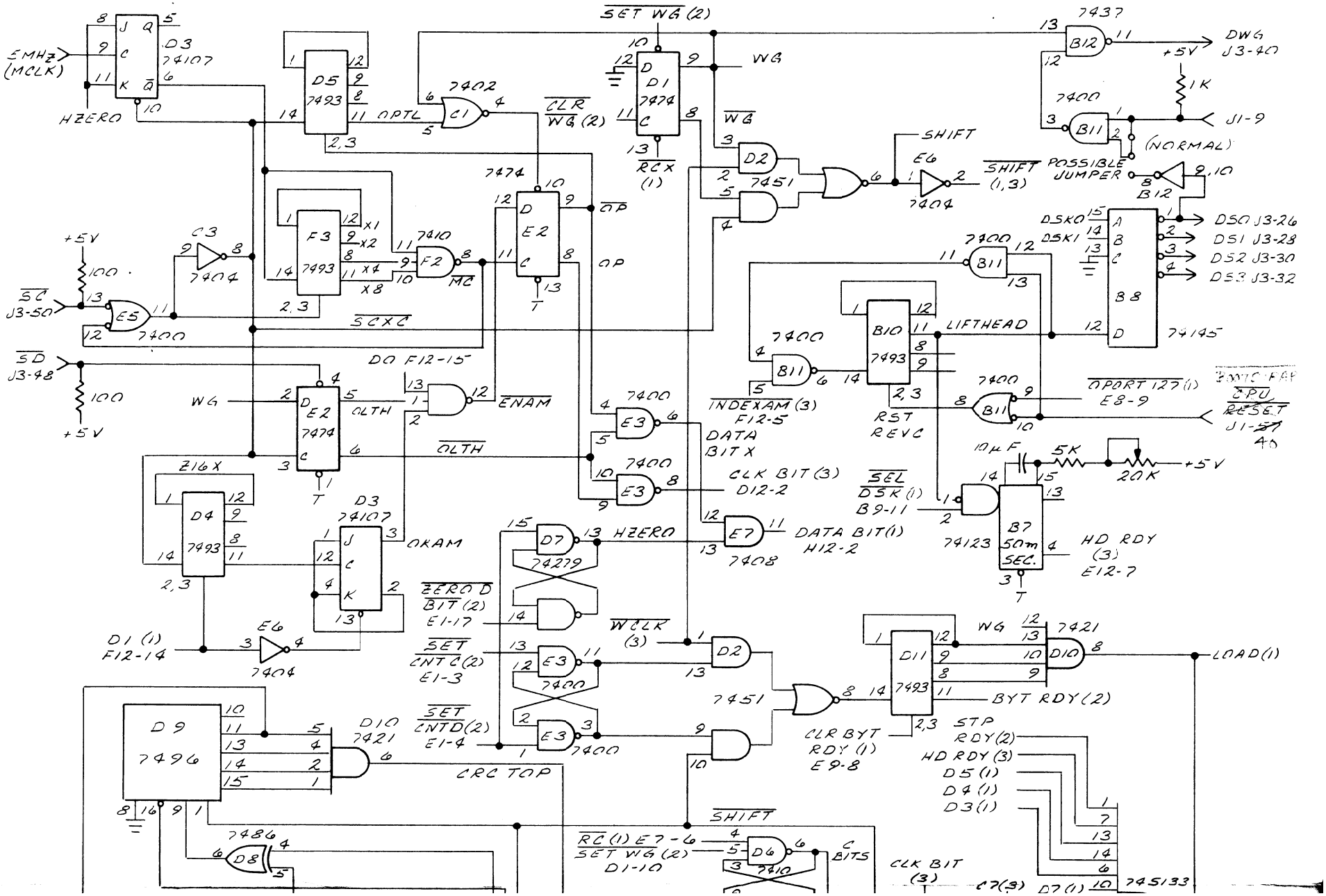
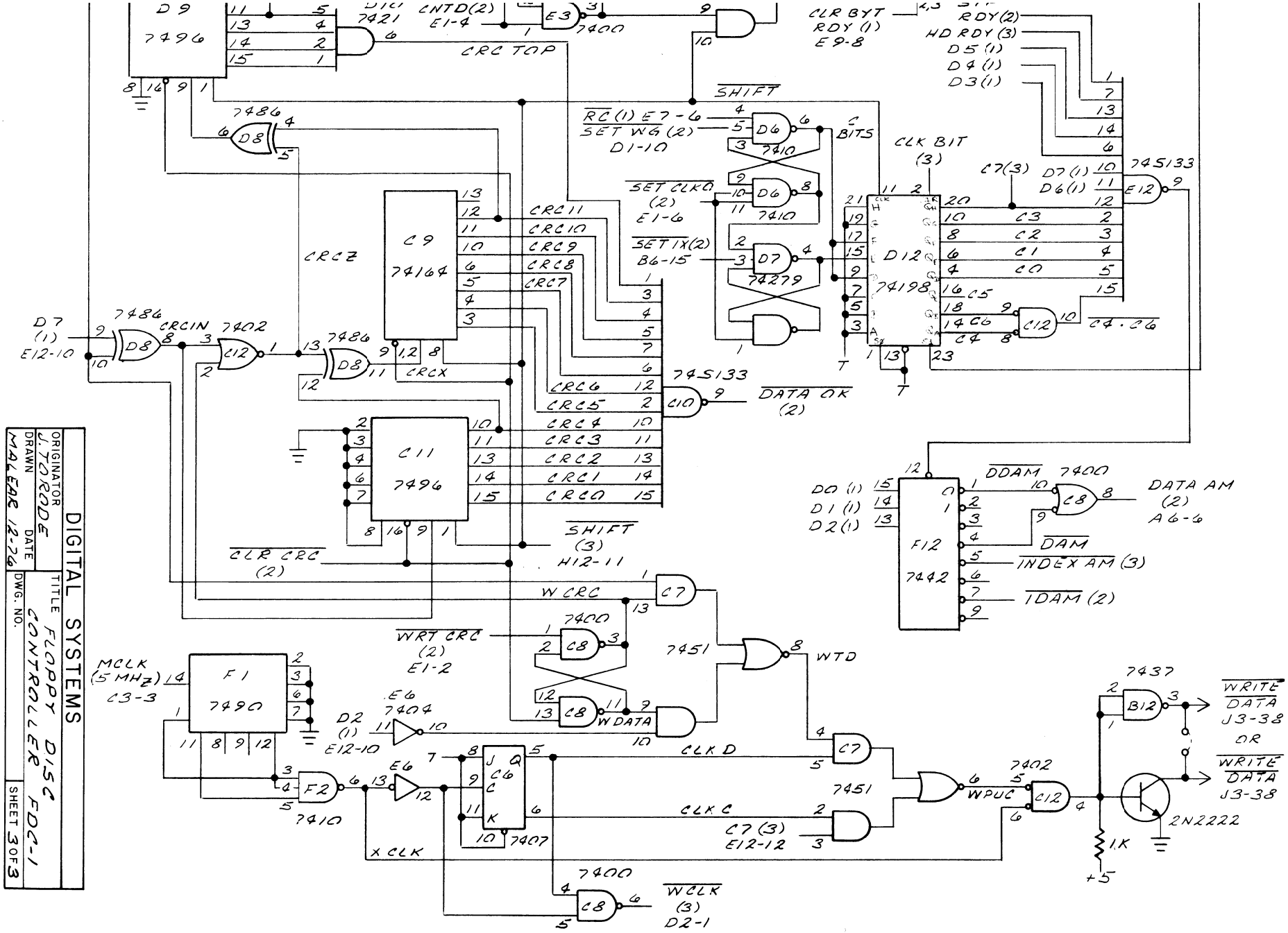
DATE 12-76
TITLE FLOPPY DISC CONTROLLER FDC-1
DWG. NO.
SHEET 2 OF 3


5MHz (MCLK)
HZERO
D3 74107
D5 7493
OPTL
C1
7402
SET WG (2)
CLR WG (2)
D1 7474
RCX (1)
WG
D2
7451
SHIFT
E6
7404
SHIFT (1,3)
POSSIBLE JUMPER
(NORMAL)
B12
7437
DWG J3-40
+5V
1K
7400
B11
J1-9
DSK0
DSK1
B8
74145
DS0 J3-26
DS1 J3-28
DS2 J3-30
DS3 J3-32
LIFTHEAD
B10
7493
RST REVC
INDEXAM (3) F12-5
OPORT 127 (1) E8-9
CPU RESET J1-40
SC J3-50
100
C3
7404
E5
7400
SCXC
F3
7493
X1
X2
X4
X8
F2
7410
MC
E2
7474
OP
T
SD J3-48
DO F12-15
WG
OLTH
ENAM
Z16X
D4
7493
OKAM
DATA BIT X
CLK BIT (3) D12-2
DATA BIT(1) H12-2
E7
7408
E3
D7
74279
HZERO
ZERO D BIT (2) E1-17
SET CNTC (2) E1-3
SET CNTD (2) E1-4
WCLK (3)
D1 (1) F12-14
10μF
5K
20K
SEL DSK (1) B9-11
B7
74123
50m SEC.
HD RDY (3) E12-7
D11
7493
7421
D10
LOAD (1)
BYT RDY (2)
CLR BYT RDY (1) E9-8
STP RDY (2)
HD RDY (3)
D5 (1)
D4 (1)
D3 (1)
D9
7496
D8
7486
CRC TOP
RC (1) E7-6
SET WG (2) D1-10
D6
7410
C BITS
CLK BIT (3)
D7 (1)
74S133



DIGITAL SYSTEMS

ORIGINATOR J. TORODE

DRAWN MALEAR 12-76

DATE

TITLE FLOPPY DISC CONTROLLER FDC-1

DWG. NO.

SHEET 30F3

INTRODUCTION

This manual provides the information needed to utilize the DIGITAL SYSTEMS Model FDC-1 floppy disk controller within a data system. It is intended as a reference for technical personnel engaged is the specification, design, and implementation of a digital system with flexible disk drive storage devices. Both hardware and software requirements for integrating the FDC-1 with memories, processors, disk drives, and system wide controlling devices are described.

Details of the interior of the FDC-1 do not appear here; these are found in the FDC-1 Technical Description manual. Aspects of the controller detailed here include specification and timing for all exterior interface signals, physical layout, power requirements, and required command sequences generally supplied under program control from a host processor system to the disk controller.

A block diagram of the FDC appears in Figure 1.

The FDC-1 is a flexible disk drive controller for up to four selectable drives. The FDC-1 uses a high speed microprocessor based design providing reliable and flexible functions implemented in read-only memory logic. Features of the FDC-1 include drive write protect, automatic CRC generation and check, full IBM 3740 compatible soft sector formatting, automatic track seek verify, and head retraction after eight idle disk rotations to assure long diskette life. An automatic bootstrap load from Track 0, Sector 1 can be done at system initialization without system processor intervention.

The FDC-1 is fully TTL implemented and compatible. An adaptible, simple interface to mini and microprocessor systems is provided with 8 bit parallel input and output busses for control information. A DMA interface moves data directly in or out of memory once a transfer is initiated.

Packaging is on a single 10" x 12" PC board with system interface via standard edge connectors and flat cable to the flexible disk drives.

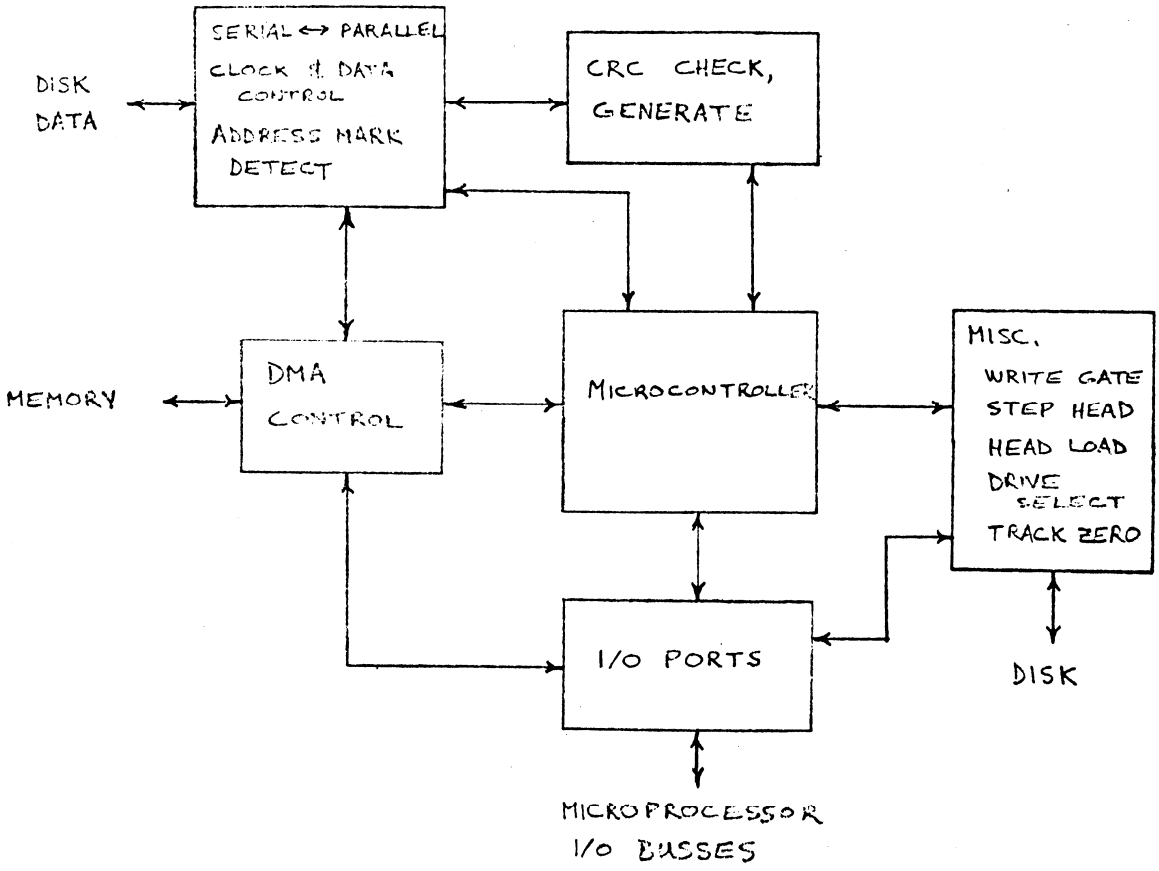


Figure 1. FDC-1 Block Diagram.

HARDWARE INTERFACE TO THE FDC-1

A diagram of the FDC external signals appears in Figure 2. The signals can be divided into three distinct interfaces; the device, direct memory interface (DMA), and disk interfaces. The device interface implements command and status information between host system control hardware (i.e. processor and processor support logic) and the FDC. The DMA interface exchanges data with up to 64 Kbytes of random access memory. The disk interface connects the FDC to a chain of flexible disk drives handling IBM format compatible diskette media. Initialization and power supply lines complete the FDC requirements.

A detailed description for each interface follows. Reference is made to the appendices containing backplane signal pinouts (J1 and J2), connector pinouts for the disk interface (J3), and the following table summarizing the mnemonic name, active state, and description for all interface signals.

Following is a summary of the busses and controls for the FDC, their names, active state, and description. All busses except MAD are 8 bits wide, bit 7 is the most significant bit, bit 0 the LSB. Index x varies from 0 to 7 unless otherwise noted.

Name	Active	Description
DINx	hi	device input bus data to host via backplane
-DOUTx	low	device output bus data from host via backplane
MDINx	hi	memory data in data to memory via backplane
MDOUTx	hi	memory data out data from memory via backplane
-DEVx	low	device address to devices
MADx	hi	x ranges from 0 to 15 16 bit memory address bus to memory via backplane
REQ	hi	single line raised by FDC to request a memory cycle
ACK	hi	single line raised by host memory system to grant a memory cycle
-WRITE	low	lowered after cycle is granted if FDC wishes to write to memory
-IN	low	input device strobe
OUT	high	output device strobe
-IRESET	low	system restart signal
-IOF	low	I/O finished by FDC
-BOOTSTRAP	low	forces FDC to execute bootstap and return -IOF
DZPROT	high	inhibit writing on disk 0

All bus levels are TTL standard, with low level signals below 0.4 VDC and high level signals above 2.5 VDC. All signals listed above except REQ and the last six signals in the table are implemented as high impedance (TRI-STATE) drivers which may be shared by other host system devices using appropriate strobing.

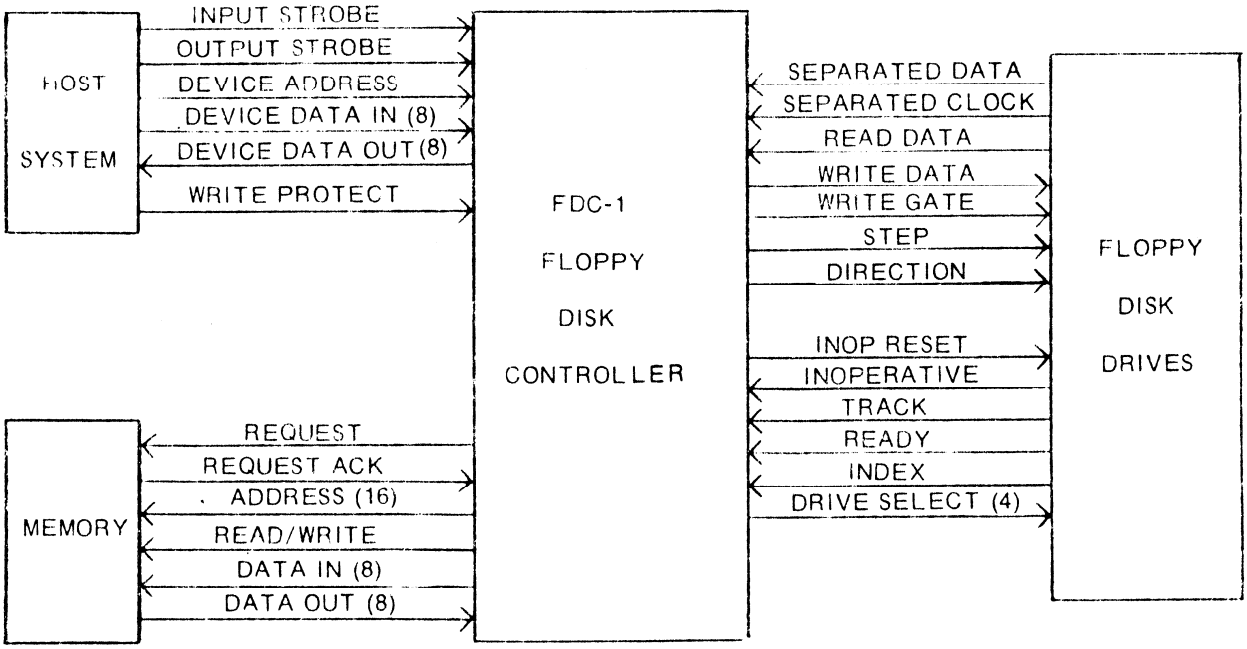


Figure 2. FDC-1 External Signals.

DEVICE INTERFACE

Interaction between the host processor or controlling hardware and the FDC is implemented by the device interface. The controller is idle until an eight bit address appears on the device address bus (-DEVi) and one of two strobes (OUT or -IN) appears simultaneously with the device address. Strobes cause decoding logic to sense the state of the -DEVi bus and, if it is presenting one of the set of addresses given below with the appropriate strobe, a set of actions occurs. With a device address and an OUT strobe, data bits present on the device output bus (-DOUTi) will affect the FDC as indicated below. Device addresses decoded with -IN will cause the FDC to drive status bits onto the device input bus (DINi) for use by the host system. All signals must be stable at their active level for a minimum of 200 nanoseconds.

Note the locations of the device address bus (-DEVi), device input bus (DINi), device output bus (-DOUTi), and strobes OUT and -IN on the table in Appendix I.

Device 127D (177Q, 7F hex) is the status input device when strobed by -IN and the command output device when strobed by OUT. The status device delivers eight bits of disk system status to the device input bus bits 0 through 7. These bits will be stable 100 nanoseconds after the device address is available and remain stable for as long as the address and strobe are stable.

The status bits are:

Bit Ø: file inoperative - an error signal from the disk indicating invalid writing sequencing

1: step ready - indicates 1Ø milliseconds elapsed since the last step command was executed and the disk is able to execute further commands

2: track zero - indicates that the read/write head on the selected disk is positioned at the outermost track

3: I/O finish - indicates that the FDC has completed processing (or aborted because of an error condition) the previous read or write command

4: track error - indicates the byte read from memory at the initial DMA address did not match the track byte of an ID field actually read from the disk. The current command is aborted.

5: ID CRC error - a CRC error was encountered in the ID field of the requested track/sector. Read commands will complete but Write commands are aborted.

6: Data CRC error - indicates a CRC error in the data fields during a Read command

7: Head Unloaded - indicates at least eight revolutions of the disk have occurred since the last Read or Write command, and the hardware has unloaded the head of the selected disk. If a software error results in a request for a sector number greater than 26D, this bit and a zero bit 3 (I/O never finishes) will indicate the error as the FDC will search forever for the requested illegal sector.

When device address 127D appears with the OUT strobe, the bits on the device output bus (-DOUTi) are interpreted by the FDC as command bits. The command register in the FDC is loaded using OUT as a strobe to the register.

Multiple bit indications are:

Bits 4,5: No data address mark was found between ID fields

Bits 4,6: Data overrun-means DMA was too slow.

The command bits are:

Bit 0: file inoperative reset - required response to the file inoperative status bit

1: step - commands the selected drive to move in the direction selected by bit 2.

2: direction - directs the disk drive to step towards Track 77 (innermost) when active (-DOUT2 low) and towards Track 00 when inactive (-DOUT2 high).

3: enable - enables loading of drive select bits 4 and 5

4: drive select - low order of two decoded select bits

5: drive select - high order of two decoded select bits. Bits 4 and 5 are latched and decoded to select one of four drives as the recipient of all commands directed to the FDC system. If bit 3 (enable) is inactive, bits 4 and 5 are ignored in a command word and the previously selected drive is used.

6: Read - initiate reading. The address of the memory buffer has been preloaded into the FDC memory address register (see below) and the host system has positioned the selected disk at the desired track. The Read command causes the first byte of the buffer to be fetched and compared to the track ID read from the drive. A mismatch causes a Track error. The second byte of the buffer is fetched and specifies a Sector number and the FDC reads sector ID fields until a match occurs. The third buffer byte is loaded by the FDC with the address mark for the data field read, then 128 bytes are transferred from the drive to memory.

7: Write - initiates a write operation. Track and sector are identified as for a Read and a Track error aborts the operation. After positioning, using track and sector bytes from the memory buffer, the third byte is written as the address mark for the data field and the next 128 bytes transferred from memory to the drive.

Note that all bits, except disk select bits, are reset on the FDC at the completion or abort of a Read or Write command. All bits are cleared when the controller is reset (-IRESET, below).

Device address 125D (175Q, 7D hex) is decoded and made available to the host system on J1-56 as signal -IN125 whenever it is issued with the -IN strobe. It is suggested that the host system use the signal as a software issued restart command by implementing the logic equivalent of Figure 3. A further explanation of Figure 3 appears in the section on initializing the FDC below.

Device address 126D when strobed by the OUT signal loads the contents of the -DOUTi data bus into the most significant byte of the DMA address register. Data on the -DOUTi bus should be stable when the OUT strobe is issued.

Device address 125D (175Q, 7D hex) when strobed by the OUT signal loads the contents of the -DOUTi data bus into the least significant byte of the DMA address register.

In summary, the device interface provides address bits to activate the FDC, uses strobes -IN and OUT to synchronize the actions of the controller with a host system, and has data paths for status and control information. These paths are used by the FDC as follows:

STROBE	ADDRESS	HOST DATA IN	HOST DATA OUT
OUT	127D	none	command word
OUT	126D	none	MSByte DMA address
OUT	125D	none	LSByte DMA address
-IN	127D	status	none
-IN	125D	none	none (J1-56: -IN125)

DMA INTERFACE

The DMA interface communicates directly with any compatible random access memory once a Read or Write command is initiated by the host system. This interface uses the DMA address register loaded by OUT devices 126D and 125D as a starting address and always employs 131 sequential bytes of memory for a disk transfer. When the FDC is ready to access memory for any single byte transfer, signal REQ (J2-55) is raised. Nothing occurs until signal ACK (J2-56) appears true, raised by the host memory system when a memory cycle is granted to the FDC. ACK should be raised within (30 - memory cycle time) microseconds of the leading edge of REQ in order to service the FDC in time. ACK must remain true during the entire memory cycle.

When ACK appears high at the FDC, REQ is lowered and the DMA address register is gated to the memory address bus MADi, and signal -WRITE is lowered if a memory write (disk read) is requested. Address lines are stable within 100 nanoseconds of the leading edge of ACK. If -WRITE remains high, a memory read (disk write) is in progress. For memory read, the host memory must gate the contents of the memory byte addressed by MADi onto the memory data out bus MDOUTi (8 bits). When the data is stable, signal ACK must be lowered. The trailing edge of ACK is used by the FDC to latch the data byte. Busses are then released by the FDC within 50 nanoseconds of the trailing edge of ACK.

If a memory write is requested, the memory address is also gated to the MADi bus when ACK appears. In addition, -WRITE is lowered and data to be written in memory is placed on the memory data input bus MDINi (8 bits). Once the host memory has captured the data and address, ACK should be lowered and the busses will be released.

The FDC requests 131 sequential bytes of data for each transfer. The first three bytes are disk address information: track number, sector number, and data address mark. The remaining 128 bytes are data. The FDC automatically increments the DMA address appropriately, formats data, and generates or checks CRC characters.

In summary, the FDC directly accesses up to 64 Kbytes of random access memory using a simple asynchronous handshaking protocol. Memory address, READ/WRITE, input data, and output data are used after a request is made and acknowledged indicating that a memory cycle is granted to the FDC. Memory buffers of 131 bytes are required for each transfer.

DISK INTERFACE

The disk interface is a set of signals on a separate 50 pin connector (J3) providing control and data paths to one to four drives.

A description of each available signal appears below. All are active low TTL level signals. An asterisk (*) next to the signal name indicates signals from the drive to the controller. A plus (+) indicates an optional signal not vital to the FDC operation. Refer to Appendix I for pinout of connector J3.

	Name	Description
*+	-FILEINOP	disk file inoperative - an error condition from the drive detecting illegal signal conditions during write
+	-FIR	file inoperative reset - response to the FILEINOP condition from the host system via the command byte
*	-INDEX	index pulse indicating rotating diskette is at the beginning of a track
*	-READY	ready level indicating drive is in an operable condition(door closed, diskette up to speed, etc.)
	-DSØ	disk select Ø - disk select lines are wired one line per drive
	-DS1	disk select 1
	-DS2	disk select 2
	-DS3	disk select 3
	-DIR	direction - indicates direction head should move in response to a -STEP pulse. A low (active) on -DIR indicates stepping toward diskette center, a high towards diskette edge (Track Ø).
	-STEP	step - 1Ø microsecond pulse to drive when a head step in the indicated direction is required
	-WRITEDATA	interleaved clock and data pulses to be written onto diskette
	-WG	write gate - signal windowing WRITEDATA to enable drive for writing
*	-TRKZRO	track zero - active when drive detects head positioned at track ØØ
*+	-READATA	interleaved data and clock pulses from drive
*	-SD	separated data pulses from drive
*	-SC	separated clock pulses from drive

The FDC requires that the drive electronics provide clock pulses on the -SC line and data pulses without clocks on the -SD line. -READATA is unused. The -STEP pulse may be longer than 1Ø microseconds.

INITIALIZATION

The sample circuitry in Figure 3 illustrates the initialization requirements for the FDC. System wide reset circuitry should place a TTL low signal (-IRESET) on J1-55 to the FDC and preset signal BOOTSTRAP. Active low -BOOTSTRAP must be available to the FDC on J1-57. When the FDC completes its bootstrap procedure of reading track zero, sector one into DMA addresses 00-7F hex, it will issue 50 nanosecond pulse -IOF . In fact, -IOF is issued at the completion of every disk input or output operation. -IOF is used to clear the BOOTSTRAP latch which in turn may be used to signal the host system to begin execution of the bootstrap program now in low memory. BOOTSTRAP may be invoked under program control by issuing an -IN strobe with device address 125D. Signal -IN125 will appear on J1-56 and set BOOTSTRAP on its trailing edge.

POWER SYSTEM

+5 volts DC should be wired to pins 1,2,3, and 4 of both connectors J1 and J2. 2.5 amps may be drawn by the FDC. Pins 83, 84, 85, and 86 of both connectors should be grounded. All odd numbered pins on connector J3 are grounded.

WRITE PROTECT

The FDC provides write protection for the disk drive selected by signal -DS0 or all drives(jumper selectable). In order to allow writing, the DZPROT signal on J1-9 must be grounded (TTL "0") by the host system.

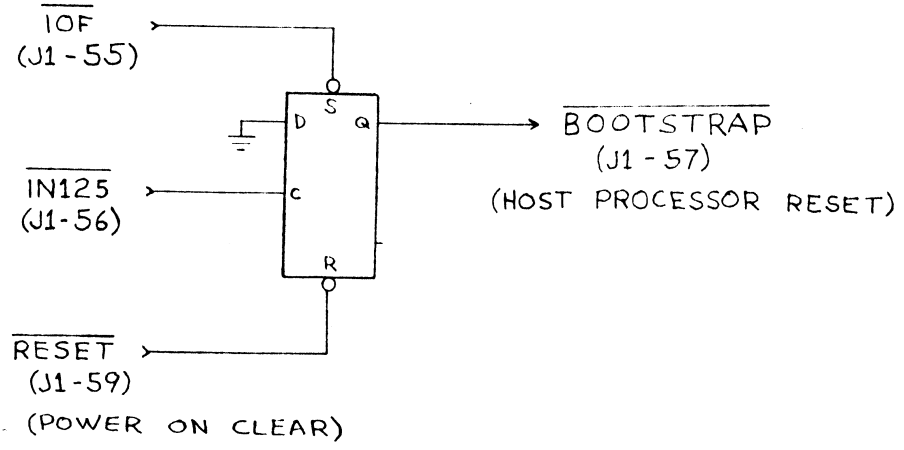


Figure 3. Initialization Circuitry.

SOFTWARE

The following system software control by the host CPU is required when using the FDC-I:

1. Software must step the head to the desired track (using STEP and DIRECTION bits of the command byte) before reading or writing.

2. The initial DMA address must be loaded (2 bytes) prior to issuing a READ or WRITE command.

3. The three bytes in memory starting at the DMA address must be set to the desired track, sector, and address mark (for write).

4. A simple retry scheme should be implemented to attempt recovery from disk errors. (For track error, seek track Ø and then desired track before retry).

Figures 4 to 7 contain flowcharts for the following routines:

HOME	-	seek track zero
STEP	-	step one track in or out
SEEK	-	seek any valid track
READ	-	read one sector
WRITE	-	write one sector

Assembly language code for the above routines is available for the 8080. Also available is a complete Disk Operating System for the 8080.

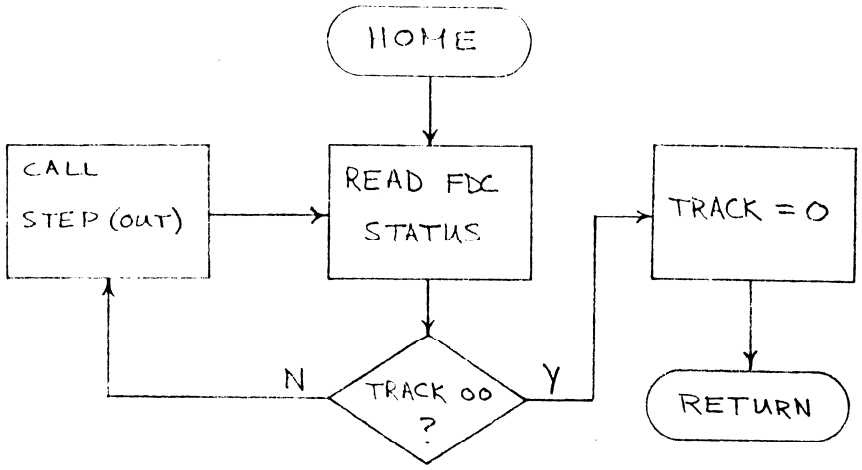


Figure 4. Subroutine HOME.

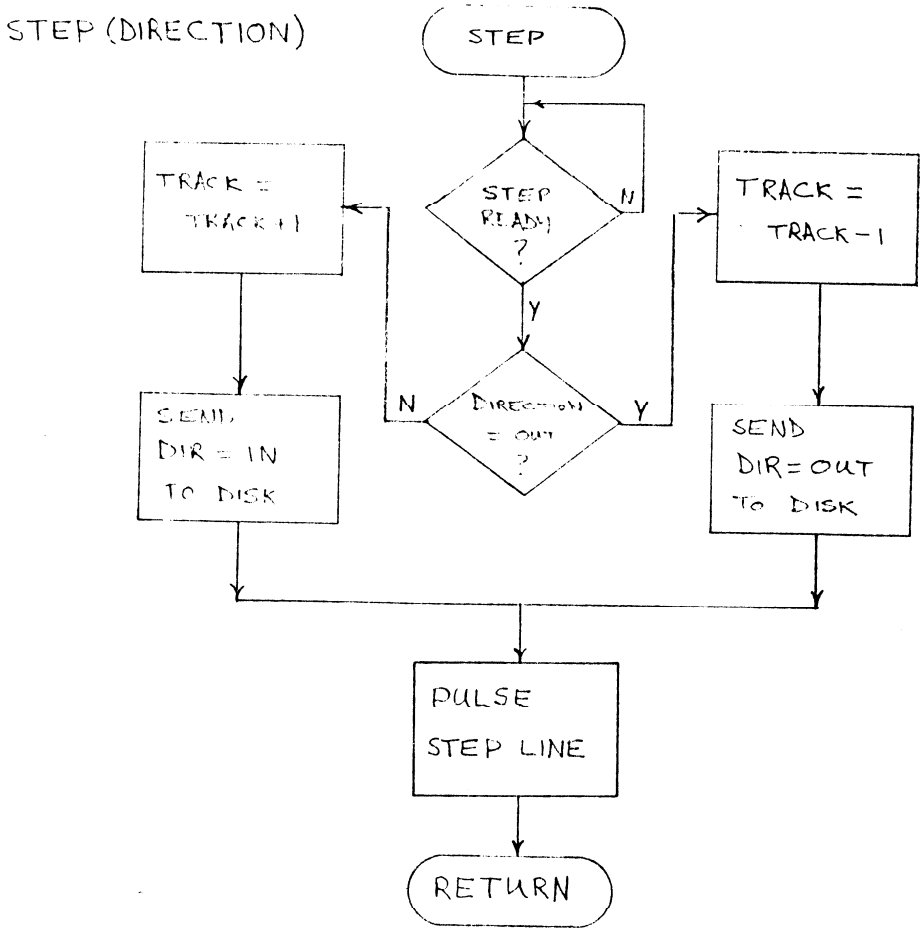


Figure 5. Subroutine STEP.

SEEK (N,ERR) MOVE HEAD TO TRACK N

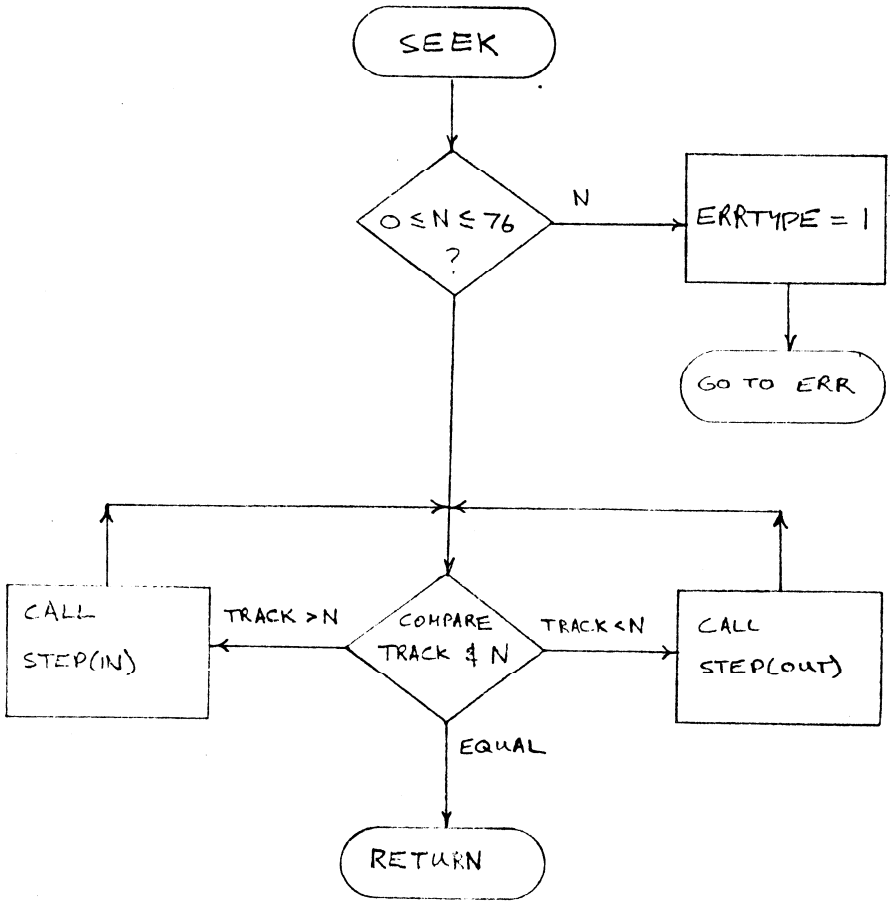


Figure 6. Subroutine SEEK.

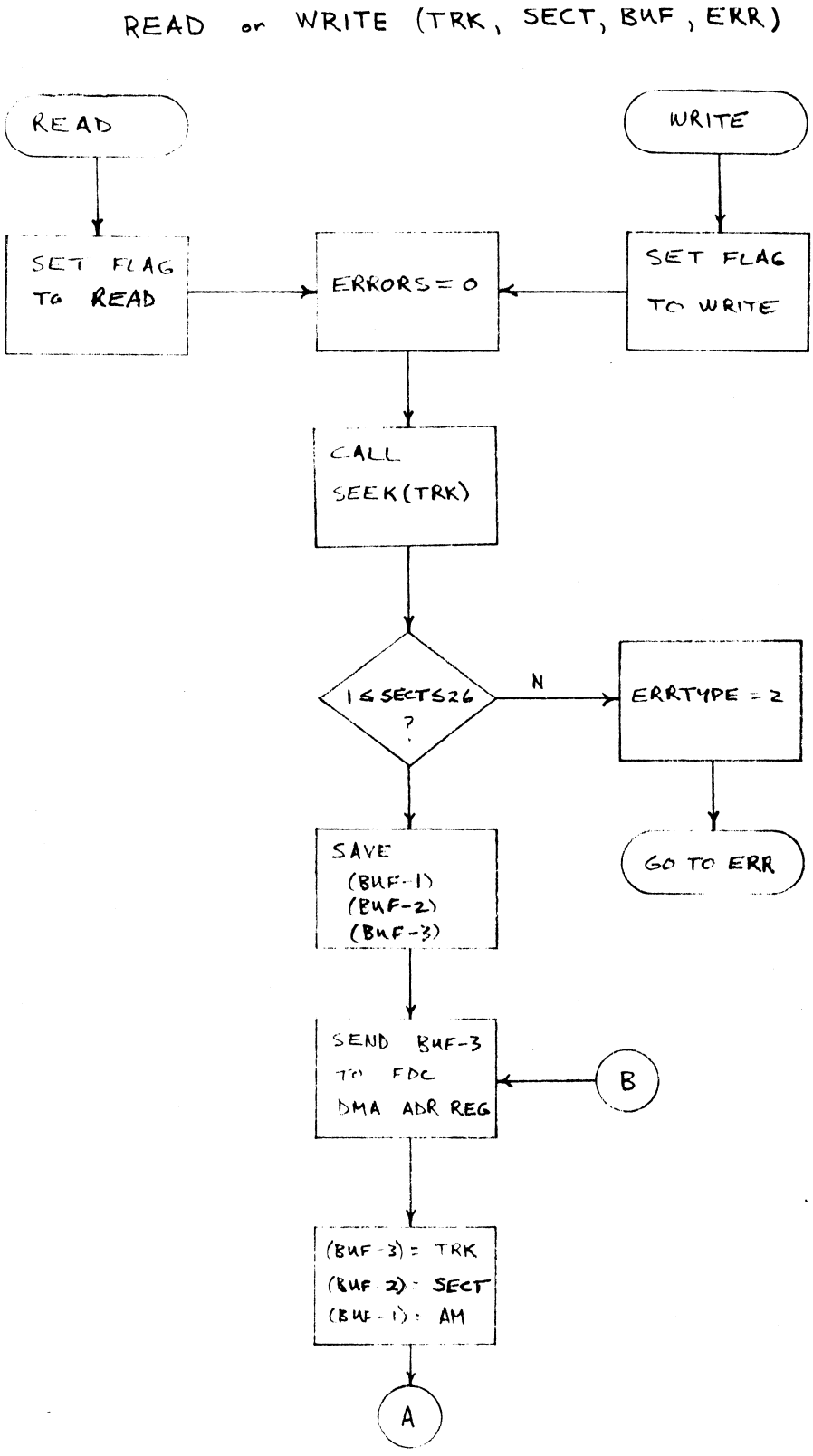


Figure 7. Subroutines READ and WRITE.

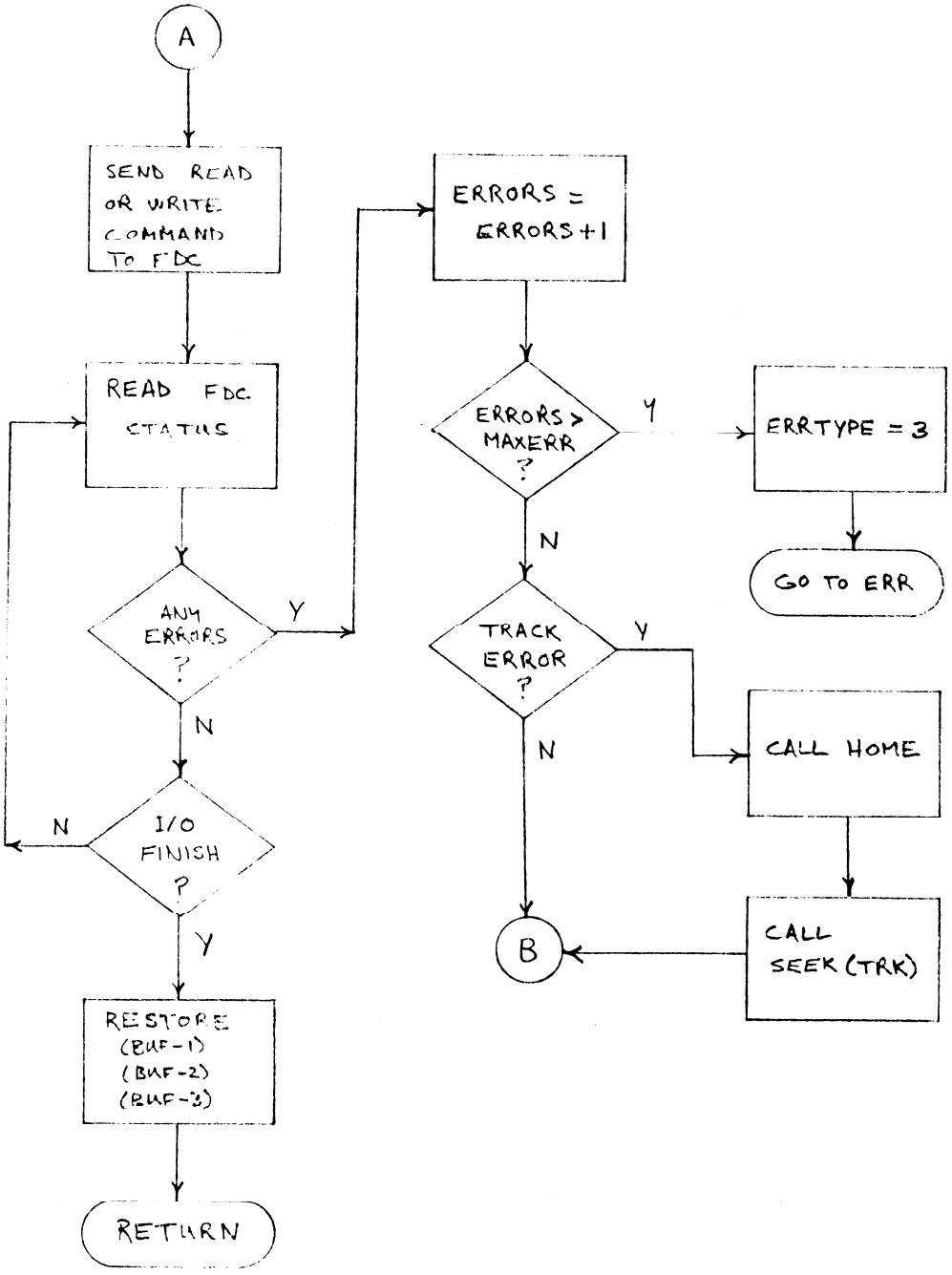


Figure 7a. Subroutines READ and WRITE (cont).

APPENDIX I EDGE CONNECTOR PINOUTS

J1 TOP EDGE CONNECTOR

1 +5 VDC	2 +5 VDC
3 +5 VDC	4 +5 VDC
5	6
7	8
9 WRITE PROT	10
11	12
13	14
15	16
17 GROUND	18 GROUND
19	20
21 -DEV0 (device address bus)	22 -DEV1
23 -DEV2	24 -DEV3
25 -DEV4	26 -DEV5
27 -DEV6	28 -DEV7
29 -DOUT0 (data out buss)	30 -DOUT1
31 -DOUT2	32 -DOUT3
33 -DOUT4	34 -DOUT5
35 -DOUT6	36 -DOUT7
37 DIN0 (data in buss)	38 DIN1
39 DIN2	40 DIN3
41 DIN4	42 DIN5
43 DIN6	44 DIN7
45 -IN (in strobe)	46 OUT (out strobe)
47	48
49	50
51	52
53	54
55 -IRESET (initial reset)	56 -IN125
57 -BOOTSTRAP	58
59 -IOF	60 -AUXROM
61	62
63	64
65	66
67	68
69	70
71	72
73	74
75	76
77	78
79	80
81	82
83 GROUND	84 GROUND
85 GROUND	86 GROUND

J2 BOTTOM EDGE CONNECTOR

1 + 5 VDC	2 + 5 VDC
3 + 5 VDC	4 + 5 VDC
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20
21 MDIN0 (memory data in)	22 MDIN1
23 MDIN2	24 MDIN3
25 MDIN4	26 MDIN5
27 MDIN6	28 MDIN7
29 MAD0 (memory address buss)	30 MAD1
31 MAD2	32 MAD3
33 MAD4	34 MAD5
35 MAD6	36 MAD7
37 MAD8	38 MAD9
39 MAD10	40 MAD11
41 MAD12	42 MAD13
43 MAD14	44 MAD15
45	46
47 MDOUT0 (memory data out)	48 MDOUT1
49 MDOUT2	50 MDOUT3
51 MDOUT4	52 MDOUT5
53 MDOUT6	54 MDOUT7
55 REQ	56 ACK
57	58
59	60
61	62
63 -WRITE (read)	64
65	66
67 GROUND	68 GROUND
69	70
71	72
73	74
75	76
77	78
79	80
81	82
83 GROUND	84 GROUND
85 GROUND	86 GROUND

J3 DISK DRIVE CONNECTOR

The controller uses a 50 connector cable for communication with the disk drives. This cable is designated J3 in the system. Pinout for the cable is:

PIN	SIGNAL NAME
2	
4	
6	
8	
10	
12	
14	
16	-FILEINOP (disk file inoperative)
18	-FIR (file inoperative reset)
20	-INDEX
22	-READY
24	
26	-DS0 (disk select 0)
28	-DS1
30	-DS2
32	-DS3
34	-DIR (direction select)
36	-STEP
38	-WRITEDATA
40	-WG (write gate)
42	-TRKZR0 (track 0)
44	
46	-READATA
48	-SD (separated data)
50	-SC (separated clock)

ALL ODD PINS: GROUND

DIGITAL SYSTEMS FDC-2

THE DIGITAL SYSTEMS FDC-2 IS IDENTICAL TO THE FDC-1 EXCEPT THAT THE INTERFACE CONNECTIONS HAVE BEEN CONSOLIDATED ONTO A SINGLE 50 CONDUCTOR FLAT CABLE (MATING CONNECTOR 3M PPART NUMBER 3415-0001).

THE TABLE BELOW GIVES THE SIGNAL NAMES AND CABLE ASSIGNMENTS FOR THE FDC-2 AND THE CORRESPONDING FDC-1 CONNECTIONS.

SIGNAL NAME	FDC-2 CONNECTION	FDC-1 CONNECTIONS			
MAD0	2	J1-21	J2-29		
MAD1	3	J1-22	J2-30		
MAD2	4	J1-23	J2-31		
MAD3	5	J1-24	J2-32		
MAD4	6	J1-25	J2-33		
MAD5	7	J1-26	J2-34		
MAD6	8	J1-27	J2-35		
MAD7	9	J1-28	J2-36		
MAD8	10	J2-37			
MAD9	11	J2-38			
MAD10	12	J2-39			
MAD11	13	J2-40			
MAD12	14	J2-41			
MAD13	15	J2-42			
MAD14	16	J2-43			
MAD15	17	J2-44			
DB0	19	J1-29	J1-37	J2-21	J2-47
DB1	20	J1-30	J1-38	J2-22	J2-48
DB2	21	J1-31	J1-39	J2-23	J2-49
DB3	22	J1-32	J1-40	J2-24	J2-50
DB4	23	J1-33	J1-41	J2-25	J2-51
DB5	24	J1-34	J1-42	J2-26	J2-52
DB6	25	J1-35	J1-43	J2-27	J2-53
DB7	26	J1-36	J1-44	J2-28	J2-54
MREQ-	28	J2-55			
MACK-	30	J2-56			
READ-	32	J2-63			
-IN-	34	J1-45			
-OUT-	36	J1-46	(NOW NEGATIVE TRUE)		
-IRESET	38	J1-55			
-BOOTSTRAP	40	J1-57			
-IOF	42	J1-59			
-IN125	44	J1-56			
-AUXROM-	46	J1-60	(LOW FOR INITIALIZATION ROMS)		
WRITEPROT	50	J1-09	(MUST BE LOW TO WRITE ON DISK)		
GROUND	1, 18, 27, 29 31, 33, 35, 37 39, 41, 43, 45 47, 49	J1-83 J2-83	J1-84 J2-84	J1-85 J2-85	J1-86 J2-86

A>